Synchronous Proximity Detection for Stretched Wire Alignment Systems

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Abstract

Suggestions are made for implementing projective/axial alignment. Electronics for reading out a stretched wire alignment system are described and a prototype design is tested with the MIT ministrip array.

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1) Defining an Axial/Projective Alignment Frame

One of the more promising alignment techniques for the GEM muon barrel[1] is the hybrid "projective/axial" concept, where 3-point optical projective monitors are used to interrelate the three superlayers at the barrel edges ($\theta = 90°$ and $30°$) and a multipoint axial monitor is used in each superlayer to define straight lines across the separate muon chamber packages stacked along the z direction. This technique, sketched in Fig. 1, was proposed in the original GEM baseline[2] and is under consideration for the cathode strip barrel[3]. Its performance has been simulated and analyzed[4,5]. This approach will eliminate the alignment gaps required between each projective tower by the conservative all-projective alignment implementation[1].

Wide-range optical alignment systems have already been prototyped[6] for the projective monitors at the barrel edges. The multipoint axial alignment scheme, however, may be realized with several different technologies; i.e. with nested 3-point optical monitors[4], stretched wire systems[3,4], and (provided care is taken in monitoring chamber rotations), proximity detectors[7].
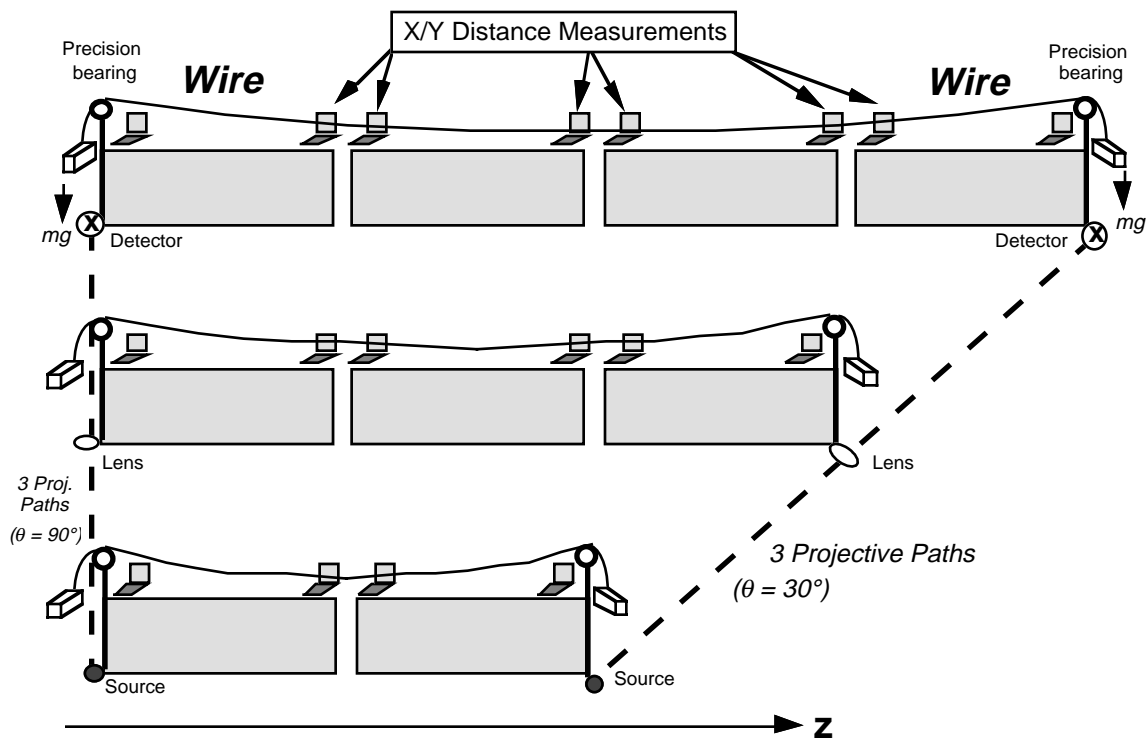

Figure 1: Hybrid axial/projective alignment using a stretched wire axial system
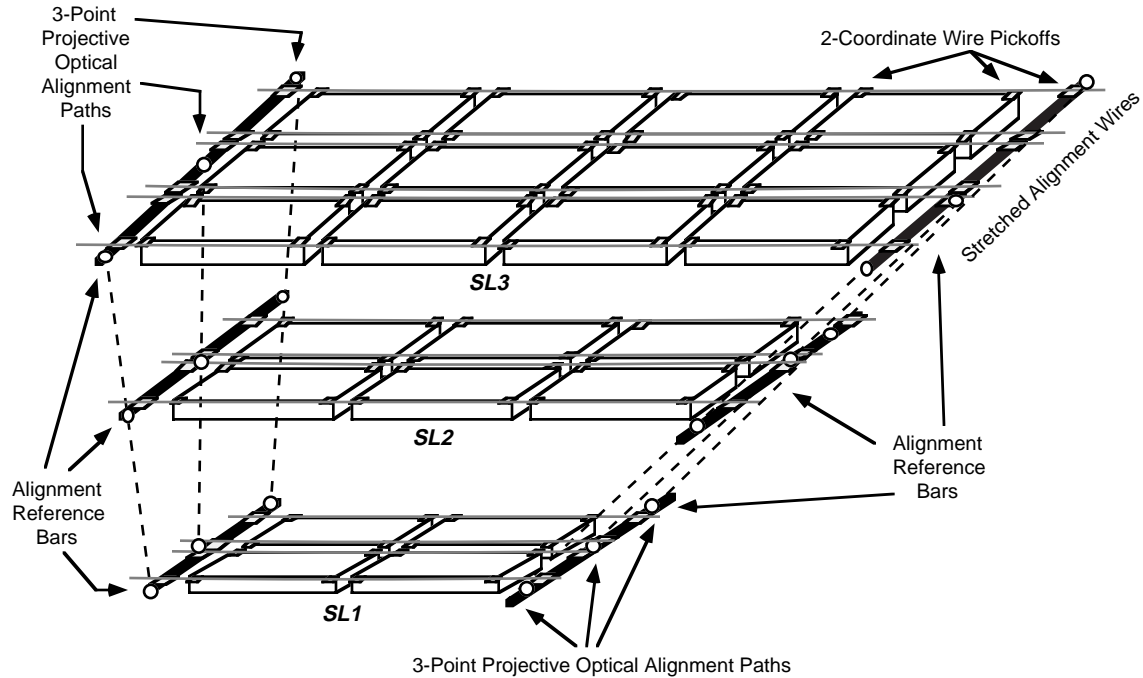
Figure 2: Axial/Projective alignment across a multi-chamber fiducial frame

In particular, the stretched-wire axial alignment scheme allows for the possibility of aligning several chamber packages together in an "alignment frame", effectively also coupling them in the ϕ coordinate. Fig. 2 illustrates this concept for a layout where each such frame includes 2 inner/middle chamber packages and 3 outer chamber packages (this is compatible with the 32/32/48 chamber segmentation that is currently under consideration by the GEM muon group). The alignment towers are 22.5° wide here, as defined by rigid alignment reference bars. A stretched alignment wire runs the length of the barrel-half along each side of a superlayer. The x and (to lower precision) y displacements of the chamber corners are measured relative to the common wire, using a dynamic measurement system such as described below. In addition, the x and y displacements of the wires are likewise monitored relative to the alignment reference bars, which also have projective optical alignment fixtures mounted on them to measure the interlayer sagitta error using quadratic interpolation[8]. The 3-layer sagitta alignment is thus transferred from the alignment bars into the wire, then back into the superlayers.

Admittedly, the implementation sketched in Fig. 2 has potential difficulties. The above-mentioned bars must be quite stiff, yet still span 22.5 deg. of phi (although introducing additional projective alignment paths along the bars should aptly describe any simple bar deflection). In addition, the superlayers are stacked across the barrel circumference, hence are not along a straight line in ϕ, as depicted in Fig. 2 (thus the bar
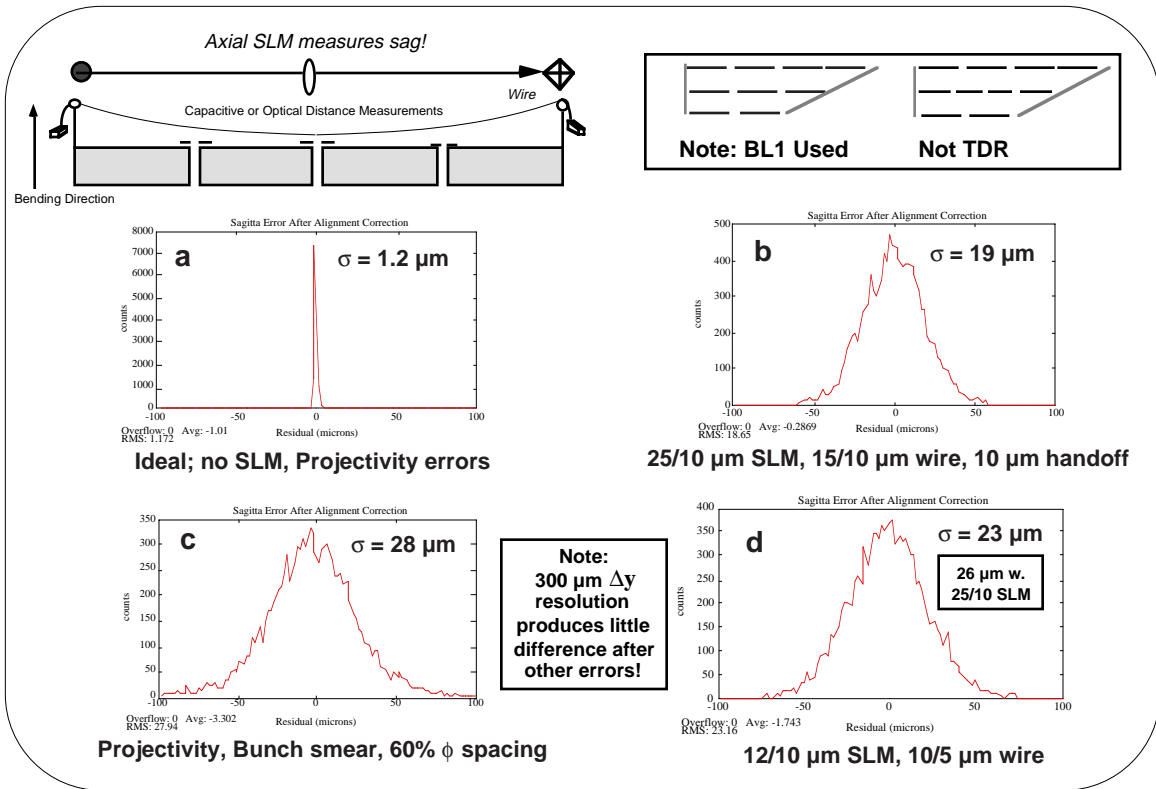
Figure 3: Error analysis for projective/axial alignment via stretched wire

should be bent/curved to follow the local circumference, or the wire pickoffs have to be on standoffs). The Lorentz-tilt of the superlayers will also prevent the ends of the stretched wires from lining up along φ. The addition of these off-chamber alignment reference bars can impact the acceptance at θ = 30° and 90°; this must be examined realistically. Fig. 2 is only intended to illustrate this concept; it depicts a naive implementation, without Lorentz-angle tilt or overlap in phi. Actual implementation will require further refinement.

An analysis[4,5] into the accuracy of a projective/axial alignment system based on a stretched wire is summarized in Fig. 3, where the sagitta error is histogrammed for muons traversing a projective/axial alignment tower (a configuration having 48 φ-towers per 2π in is assumed) with chambers given random rotations and translations within the limits established in Table 4-16 of Ref. [1]. The Baseline I "equal-length chamber" configuration is assumed. The cartoon at upper left (showing the axial optical monitor in parallel with the wire) is not employed in this analysis; it is meant to suggest a technique for monitoring the wire sag, which can amount to several hundred μm over the longest (15 meter) axial paths in GEM. Effects of sag are not included here, but must be

accounted for in practice; a method for monitoring the sag of the wire (i.e. the parallel monitor concept sketched in Fig. 3, or the standard method of determining the wire's resonant frequency) should be implemented.

The plot at upper left (a) shows the false sagitta resulting from the basic projective alignment correction[8] under ideal conditions; i.e. no noise in the alignment monitors, no beam smear, projective fixtures mounted at the chamber edges, and perfect z-coordinate chamber resolution. This is essentially the error intrinsic to the quadratic correction implicit in projective alignment, and as one can note, it's very narrow (i.e. 1.2 μm RMS). The plot at upper right (b) assumes pessimistic alignment monitor resolution; i.e. 25 μm projective monitor sagitta resolution, 15 μm stretched wire resolution, 10 μm alignment transfers (optical fixture or wire pickoff to chamber), and 10 μm projective to axial system transfer. The false sagitta here (19 μm RMS) is significantly worse. The plot at lower left (c) incorporates all other error sources; i.e. the previous monitor errors, plus a 4.25 cm beam smear (corrected[5] with the measured vertex), 1.5 cm chamber z-resolution, and the effect of mounting the projective monitors 30% inward from the superlayer edges (to allow for alignment paths with a shingled overlap in ϕ). The false sagitta has now increased to 28 μm RMS, which is above the 25 μm allowance. Finally, the plot at lower right (d) incorporates all these error sources, but uses better monitor resolutions, still in accordance with the latest test results (12 μm RMS sagitta error in the projective monitors with 10 μm alignment transfer, 10 μm stretched wire resolution with a 5 μm alignment transfer); the false sagitta now reaches 23 μm RMS, meeting the prescribed limit.

The above analysis has indicated that the 25 μm sagitta error goal can be achieved, provided the axial alignment system is capable of attaining a 10 μm position resolution with a low alignment transfer. It is known that a stretched-wire system can deliver this level of accuracy; as has been demonstrated recently[9] using the MIT mini-strip technique[3], discussed in more detail below. Since the ministrips can be etched directly onto a cathode plane, very low alignment transfers can likewise be attained. Multipoint axial alignment requires both sagitta (x) and radial (y) coordinates to be measured, although the y coordinate need be determined with much less resolution if the projective towers are narrow in ϕ (as indicated in Fig. 3, the false sagitta width was affected little after the Δy resolution was loosened to 300 μm). The ministrip alignment method fits this criterion, as it measures x precisely and delivers the y coordinate with a looser tolerance.
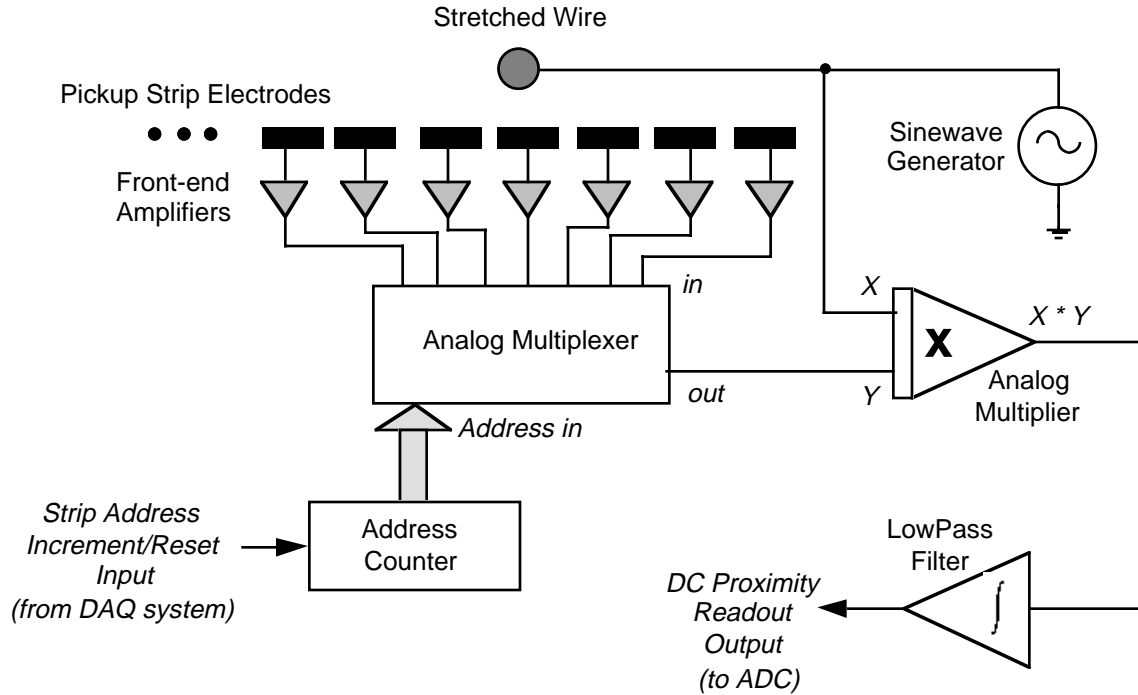
Figure 4: System used to readout ministrip array

2) Front-End Electronics for Efficient Mini-Strip Readout

A scheme to implement a stretched wire alignment detector using a pickup electrode pixelated into ministrips has been recently proposed[3], and the initial test results are extremely promising[9]. The remainder of this report describes analog readout electronics that were developed to support this approach.

Fig. 4 shows a block diagram of the suggested design, based upon a synchronous detection principle perfected at the MIT Media Laboratory[10] to track the dynamic position of a cello bow for hyperinstrument research and performance. The conductive stretched wire is driven by a sine wave, which capacitively couples into a set of pickup strips on a conventional G10 circuit card. Gain is provided by a set of low-impedance current amplifiers (one for each strip). An analog multiplexer is addressed to select the output of each preamplifier, which is then synchronously demodulated in a low-cost analog multiplier, producing components at DC and twice the oscillator frequency. The 2f component is filtered out by a simple first-order lowpass filter, and the resulting signal is a DC voltage proportional to the signal coupling, which is a function of the distance from the pickup wire to the selected strip, as was demonstrated previously[3].
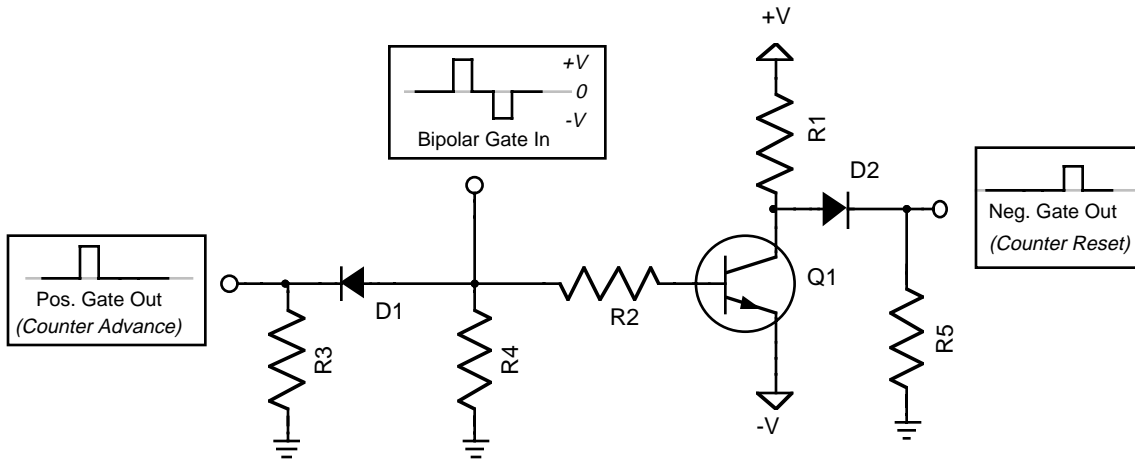
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Fig. 5: Suggestion for a bipolar gate separator circuit

Related methods have recently been suggested[11], using an identical front-end, but a narrowband filter and peak detector instead of the synchronous demodulator and low-pass filter. Although this approach will also work, the heterodyne technique of Fig. 4 has some advantages; i.e. the lowpass filter effectively implements a very narrow bandpass response perfectly centered around the oscillator frequency (rejecting the vast extraneous pickup that will be present at an accelerator facility), any convenient oscillator frequency can be chosen (hopefully minimizing crosstalk into the chamber electronics), and (in contrast to the peak-detector) the low-pass filtered output will also track the wire dynamics (provided that the cutoff is chosen above 30 Hz or so), which will be very useful in calibrating the wire tension[12].

The multiplexer will be addressed by the output of an on-card binary counter. The possibility of allowing this counter to free-run at some 10's of Hz has been discussed[13], where the demodulated output would be continuously sampled as the multiplexer repeatedly toggles through its inputs. In this case, the counter phase would be reconstructed off-line (or in a microcontroller) by using a set of "guard channels"; e.g. extra channels on the multiplexer with a non-physical DC offset that are cycled through during readout to provide synchronization of the data acquisition stream. Granted, this does remove the need for providing an external handshaking line, but it comes at a price; it will be very useful in some situations (i.e. when monitoring the wire dynamics or in a diagnostic mode) to sit at one particular channel and continuously monitor its output.

Fig. 4 sketches an alternative that can implement external control of the multiplexer address with a single cable; a positive pulse on this line will cause the counter to toggle to the next multiplexer address, and a negative pulse will cause the counter to reset to zero. The positive and negative pulses can be separated into two logic lines by

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using a simple transistor circuit as sketched in Fig. 5, which provides a logic drive easily compatible with CMOS inputs. This circuit is just an obvious suggestion; many other implementations of such a gate separator are possible, some of which may be better integrated.

The demodulated DC output must be digitized by an ADC, then the data accessed by a data acquisition system. This document doesn't deal with this topic in any depth; more discussion is given in Ref. [11], where a 12-bit ADC (analog-digital converter) is proposed to be integrated into the readout system. A suggestion has been recently made[13] to put the demodulator, lowpass filter, and ADC onto a single data acquisition card. In this fashion, the outputs from several ministrip cards (i.e. all cards in a barrel sector or along a common wire) will be multiplexed into a common demodulator/ADC circuit. This has some definite advantages; i.e. the ministrip cards will provide the multiplexer output directly (hence the induced AC signal is available directly for inspection, which will aid in troubleshooting), the oscillator signal need not be routed to each ministrip card for demodulation, and fewer components are needed.

In order to minimize risk of crosstalk into the chamber signals, the circuit used to drive the wires in the actual experiment should be programmably gated; i.e. each wire should be modulated only while data is being taken on its corresponding ministrip cards.

For testing purposes, an integrated ADC may not be necessary; the electronics of Fig. 4 can be mounted on the card with the ministrips (or built on a different card which sockets into the ministrip card), and a standard CAMAC or VME slow ADC used to digitize the demodulated outputs. A CAMAC or VME output register can provide common multiplexer addressing lines, or two such bits can be combined into one bipolar line to cycle/reset the multiplexers, as sketched in Fig. 5. One ADC channel will be required for each ministrip card; the addressing of all ministrip multiplexers can then be controlled in parallel.
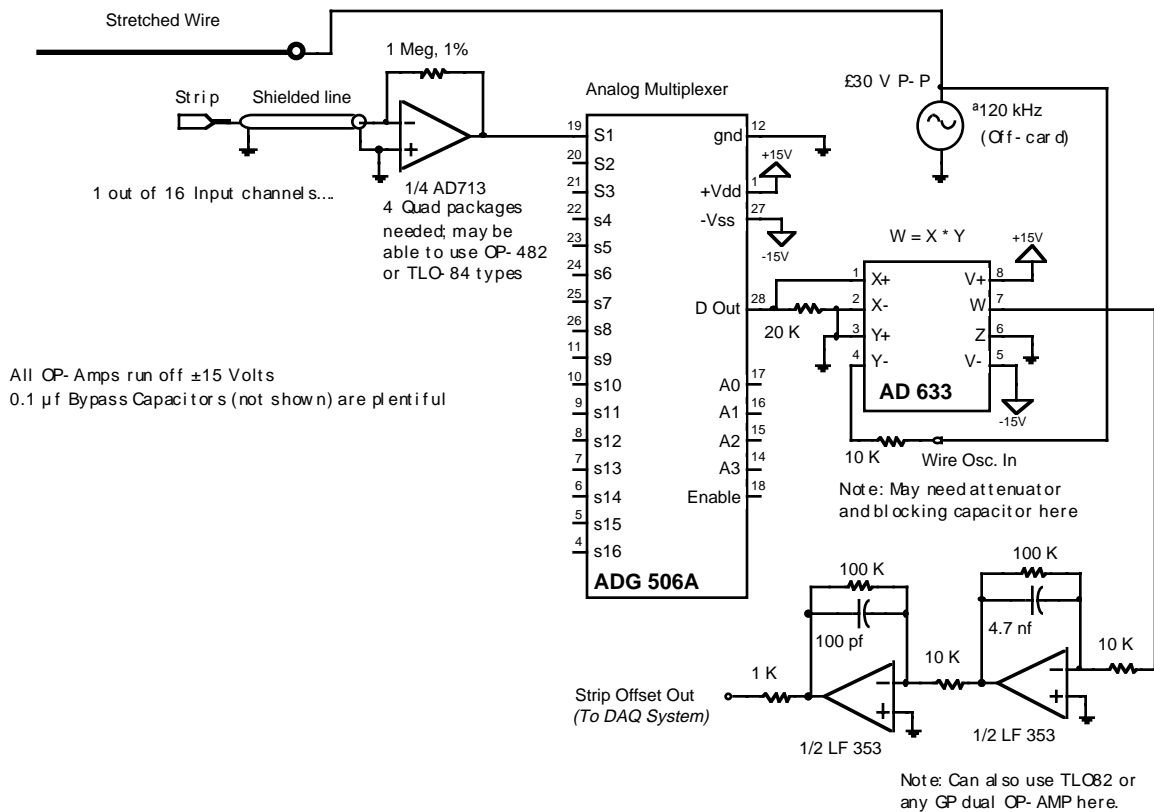
Figure 6: Analog electronics used in ministrip test

3) Test Implementation and Results

A circuit similar to the block diagram of Fig. 4 has been prototyped and tested with the ministrip setup at the MIT Bldg. 24 LNS lab. The schematic diagram for the analog electronics constructed for these tests is shown in Fig. 6. All available 16 strips were buffered and multiplexed. The strips were separated from the front-end amplifiers by roughly 2 feet of shielded coax. In a printed-circuit implementation, great care must be taken with these lines; i.e. they should either be shielded or made as short as possible to avoid common-mode (or non-strip related) pickup and crosstalk. The stretched wire was driven by the sinewave output from a common HP signal generator running at maximum amplitude (yielding 25 V P-P). The optimal oscillator frequency was found to be in the vicinity of 120 kHz; here the maximum amount of signal was coupled into the strips (coupling increases with frequency) before the phase-shift and rolloff characteristics of the input operational amplifiers began to become significant. With the

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wire roughly 1-2 mm above the strips, the maximum front-end op-amp output was seen to be on the order of 3 V p-p.

The choice of front-end amplifier isn't terribly critical here; any FET-input device with slew above 10 V/μs and decent noise characteristics will probably be adequate. The present tests employed the AD713 quad package from Analog Devices; this is a fast (20 V/μs), high-quality device popular in high-end audio applications, listing at $7. for single units and $3.50 in 500-piece quantities. It works well, but future tests will attempt to replace it with an OP-482 or TLO84 device, which are at least a factor of 4 less expensive, and will probably suffice.

One percent resistors have been chosen to set the gain of the input stage; a finer calibration will be realized *in situ* by pulsing a common orthogonal strip placed behind the ministrip card. The amplifiers in the prototype card are sufficiently AC stable without additional compensation. If they start to oscillate in a future design, the addition of a circa 2 pf feedback capacitor should provide adequate damping (the signal will be attenuated and phase-shifted, however, potentially requiring the oscillator frequency to be re-adjusted for optimum performance).

Individual strip signals were selected by a 16-to-1 analog multiplexer chip (AD506A). This chip is a 28-pin package, and runs at the full supply voltage (±15 volts), thus no biasing or decoupling is required; in addition the address inputs are fully compatible with TTL or CMOS logic levels. This device lists at $11.50 in single units, reducing to $7. for 500-piece quantities; surface-mount packages are available. A potentially less expensive multiplexer implementation has been suggested[11], using a pair of CD4051 8-channel CMOS multiplexers (quoted at $1.20 in single quantities). Since the maximum front-end output is on the order of 3 volts P-P (thus headroom isn't crucial in this application), these devices are adequate, provided the input op-amps are biased up to half the supply voltage (such CMOS devices don't operate with a supply in excess of 15 V), and the multiplexer outputs are AC-coupled into the multiplier.

The demodulation is accomplished with an AD633 low-cost 4-quadrant multiplier, which performs adequately for this purpose (the maximum error is quoted at 2% of full-scale; the mini-strips can be calibrated and employ essentially a relative measurement, hence a more precise product isn't required). This device is quite inexpensive ($5.25 for singles, $3.75 in 500-piece quantities). If the oscillator is operated beyond the supply voltage, an attenuator will have to be added to prevent the multiplier's input stage from overloading.

The final stage of Fig. 6 is a low-pass filter and 20 dB gain block, realized around a common dual operational amplifier, such as the TLO82 or OP282 (which list at $1.80
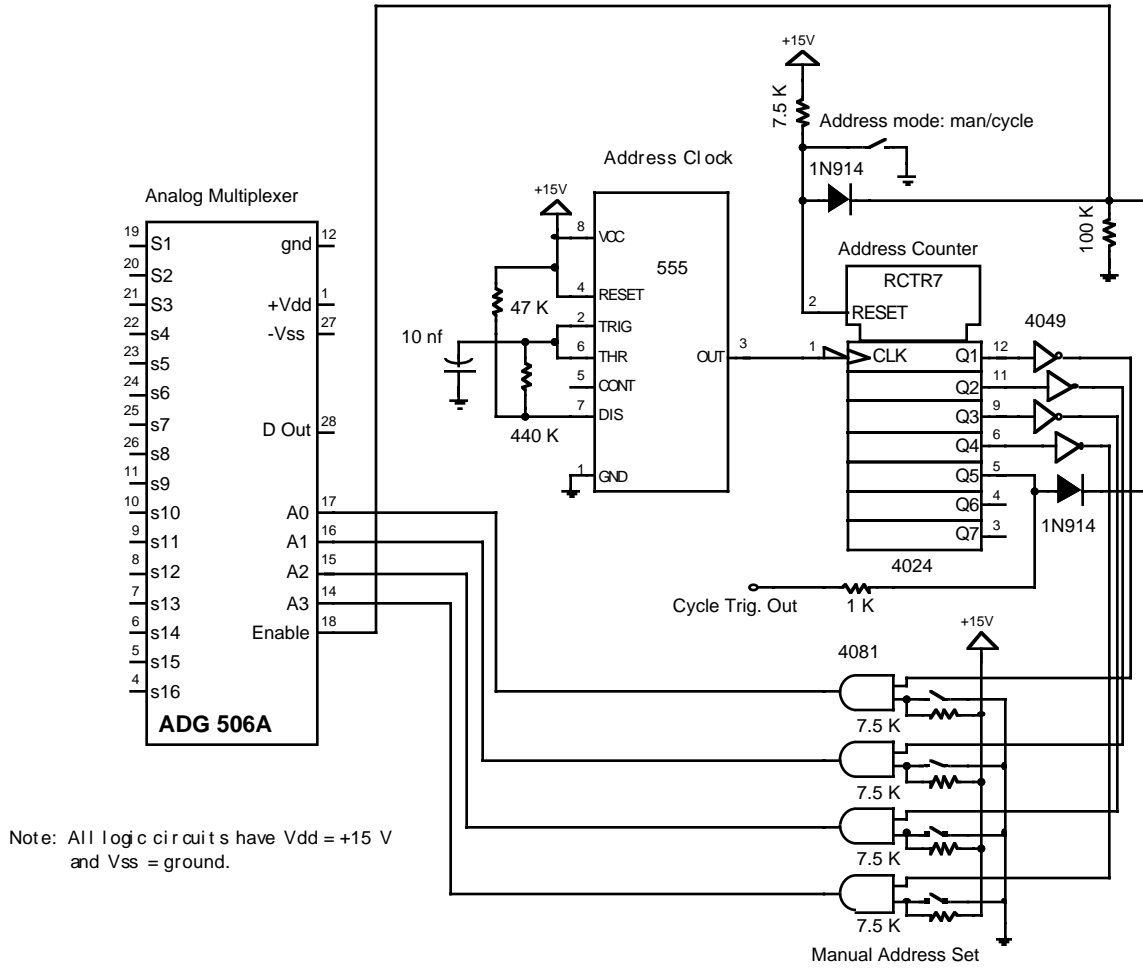
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Figure 7: Address generator for prototype test circuit

for single units and $1.20 for 500-piece quantities). The filter has a cutoff around 300 Hz, which is a little high; it could be dropped below 100 Hz (thus the capacitor could be raised to the vicinity of 15 nf), and still track the wire dynamics (which should be around 25 Hz)[3].

Fig. 7 shows the circuit that was used to address the multiplexer during the tests. A 555 timer running at 150 Hz toggles a CMOS binary ripple counter (CD4024). The four low bits are used to address the multiplexer, and the fifth bit toggles the multiplexer enable line. This causes all 16 channels to be sequentially presented at the multiplexer output, followed by an equal interval of blank signal while the multiplexer is disabled. A set of DIP switches are also provided on the prototype circuit that allow one to disable the automatic address cycling and directly access any multiplexer input. This circuit was
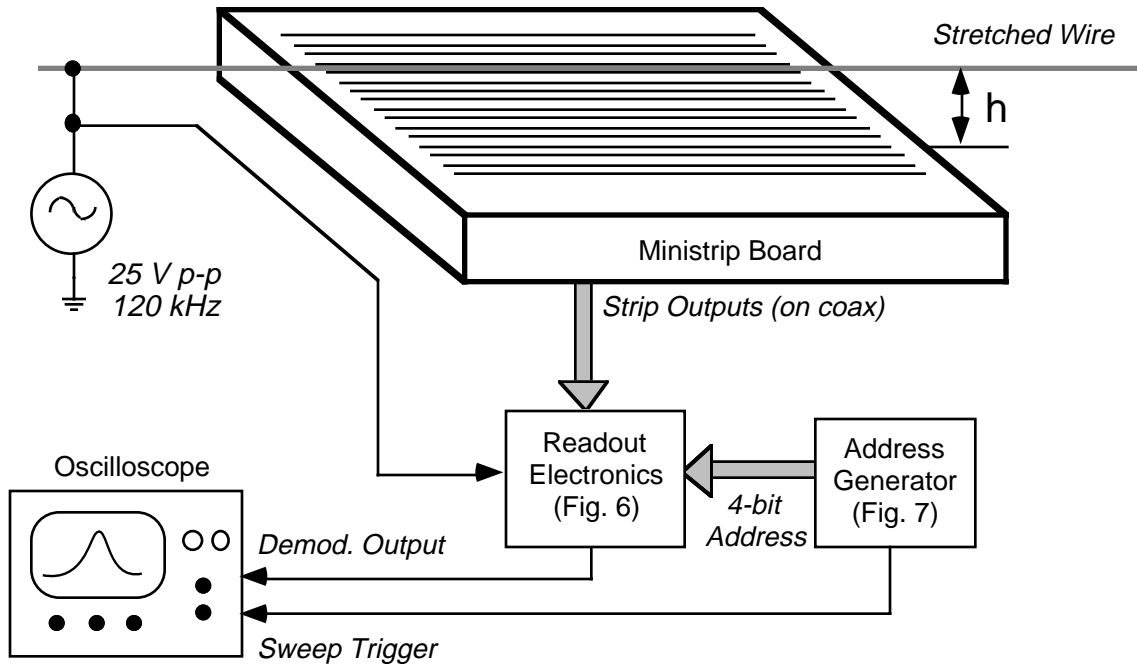
Figure 8: Test setup at MIT for verifying ministrip electronics performance

provided to aid in testing, and is not suggested for actual implementation; the necessary addressing logic was discussed in the previous section.

The electronics described above were connected to the prototype ministrip board[9] at MIT/LNS, and the demodulated DC outputs of each of the 16 strips were plotted on an oscilloscope (the strip channels were continually scanned in their layout sequence via the address generator of Fig. 7; the fifth counter bit was used as a trigger to stabilize the trace). These results are only intended to qualitatively demonstrate the electronics performance; a quantitative analysis of the ministrip accuracy is given in Ref. [9]. The test setup that was used is sketched in Fig. 8.

Fig. 9 shows the demodulated strip outputs when the wire is very close (i.e. within a millimeter or less) to the strip board. The strip readout is plotted in the center half of the trace; the flat regions at left and right edges represent the "guard" band, where the multiplexer was disabled. The horizontal sweep is at 20 ms per division in all of these photos; the edge-rounding transient seen as the multiplexer switches channels is due to the low-pass demodulation filter.

The strip output distribution is highly peaked, with most induced signal distributed between 3 or less strips. The output level is also high here (the circuit of Fig.
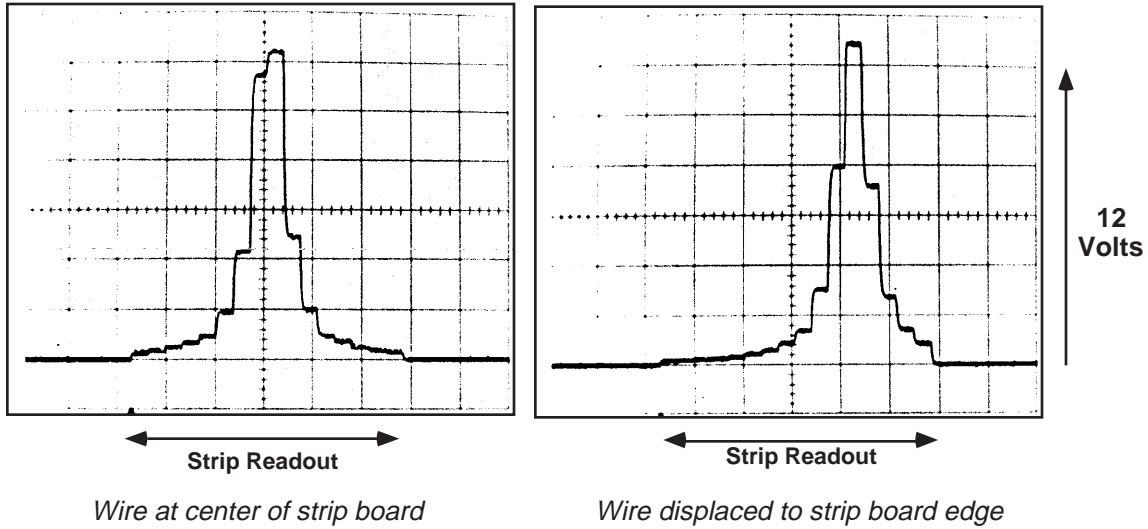
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Wire at center of strip board   *Wire displaced to strip board edge*

Figure 9: Strip voltages for stretched wire at different positions across ministrip board

6 produced a peak near 12 volts, which is approaching the saturation limit of the operational amplifiers).

The photo at left in Fig. 9 had the wire roughly centered relative to the strip board; it was displaced toward one of the edges (maintaining roughly the same vertical spacing) in the photo at right; the change in charge distribution is very clear, demonstrating the sensitivity of this alignment technique.

Fig. 10 shows the strip voltages again, but this time for arrangements with the wire at various heights (h in Fig. 8) above the ministrip board. The characteristic broadening in the width of the induced signal[3,9] is evident as the wire is moved away. The peak height also varies; Fig. 10 shows the maximum demodulator output varying from roughly 12 volts (at a 1 mm distance) down to 0.8 volts (at 1 cm). The centroid of this distribution determines the lateral position across the strip board, and its width provides a measurement of the height of the wire above the board; the decoupling of these coordinates is discussed in Refs. [3,9].

If the stretched wire is sandwiched between the ministrip board and another non-pixelated board (i.e. a flat conductive plane), the difference between the sum of ministrip outputs and the signal induced onto the opposing flat plane will provide another measurement of the height (h) without relying exclusively on the width of the induced signal. This should be considered for actual chamber implementation.

The noise seen in these tests was dominated by extraneous signal pickup at frequencies ranging between 500 kHz and several MHz. This was nonetheless relatively small (i.e. it appeared at the level of 10 mV p-p), and was independent of the driving
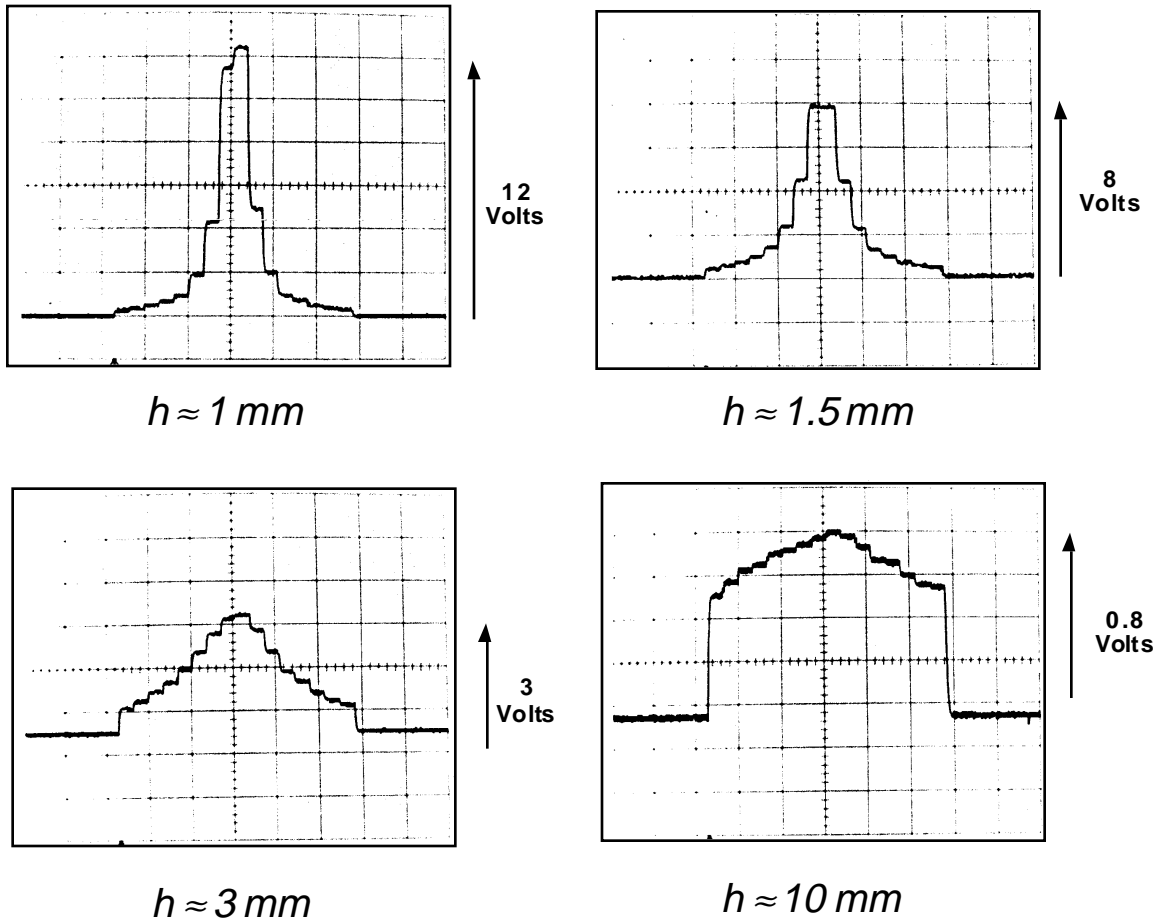
$h \approx 1\,mm$ 12 Volts

$h \approx 1.5\,mm$ 8 Volts

$h \approx 3\,mm$ 3 Volts

$h \approx 10\,mm$ 0.8 Volts

Figure 10: Strip voltages for stretched wire at different heights above ministrip board

oscillator. It was most probably induced over the power supply lines and ground, and can be easily avoided; this circuit is capable of attaining a significantly lower noise floor.

Conclusions

A multiplexed synchronous readout of the ministrip alignment system has been successfully tested. The design is very simple and inexpensive; the analog readout components will cost in the vicinity of $25. per board in single unit quantities (dropping by roughly half for over 500 pieces). Suggestions were given for streamlining this design, incorporating it into a data acquisition architecture, and implementing it both in future tests and at the GEM detector.

Acknowledgments

References

[1] "GEM Technical Design Report," Chapter 4, GEM-TN-93-262.

[2] Paradiso, J., "Some Alignment Concepts for the GEM Muon Array,"
GEM-TN-92-124, June, 1992.

[3] Korytov, A., "The Axial + Projective Alignment for Muon Chambers,"
GEM TN-93-302, March, 1993.

[4] Paradiso, J., "Analysis of an Alignment Scheme for the GEM Muon Barrel,"
GEM-TN-92-150, October, 1992.

[5] Paradiso, J., "More Muon Alignment", presented at the GEM Muon Review
Meeting - SSCL, June 30, 1993, GEM TN-93-433.
Paradiso, J., "Alignment Analysis", presented at the GEM SSCL/Muon Meeting -
San Diego, CA., May 11, 1993, GEM TN-93-415.

[6] Paradiso, J., Goodwin, D., "Wide-Range Precision Alignment For The Gem Muon
System", presented at the Third International Accelerator Alignment Conference,
Annecy, France, Sept. 28 - Oct. 1, 1993.

[7]   Antebi, J., Zarghamee, M., "Monolithic Integrated Concepts for Muon Subsystem Structures", SGH presentation/report Comm. 93095, SGH Corp., Arlington, MA. June 8, 1993.

[8]   Mitselmakher, G. and Ostapchuk, A., "New Approach to Muon System Alignment," GEM TN-92-202, October 1992.

[9]   Korytov, A., to be published in the Proc. of the Third International Accelerator Alignment Conference, Annecy, France, Sept. 28 - Oct. 1, 1993.

[10]   Gershenfeld, N., "Sensors for Real-Time Cello Analysis and Interpretation", Proc. of the ICMC, Montreal, Canada, 1991.

[11]   Marlow, D., "Wire Alignment Readout Electronics", Princeton/GEM internal memo, July 27, 1993.

[12]   Ahlen, S., et. al., "Wire Positioning Accuracy Based on Knowledge of Wire Tension", GEM TN-92-74, Feb., 1992.

[13]   Marlow, D., personal and Internet communication, August, 1993.