Compilation of Data on the Current TEC Analog Electronics

--- J. Paradiso
Oct., 1983

COMPILATION OF DETAILS ON CURRENT TEC ANALOG ELECTRONICS

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CONTENTS......

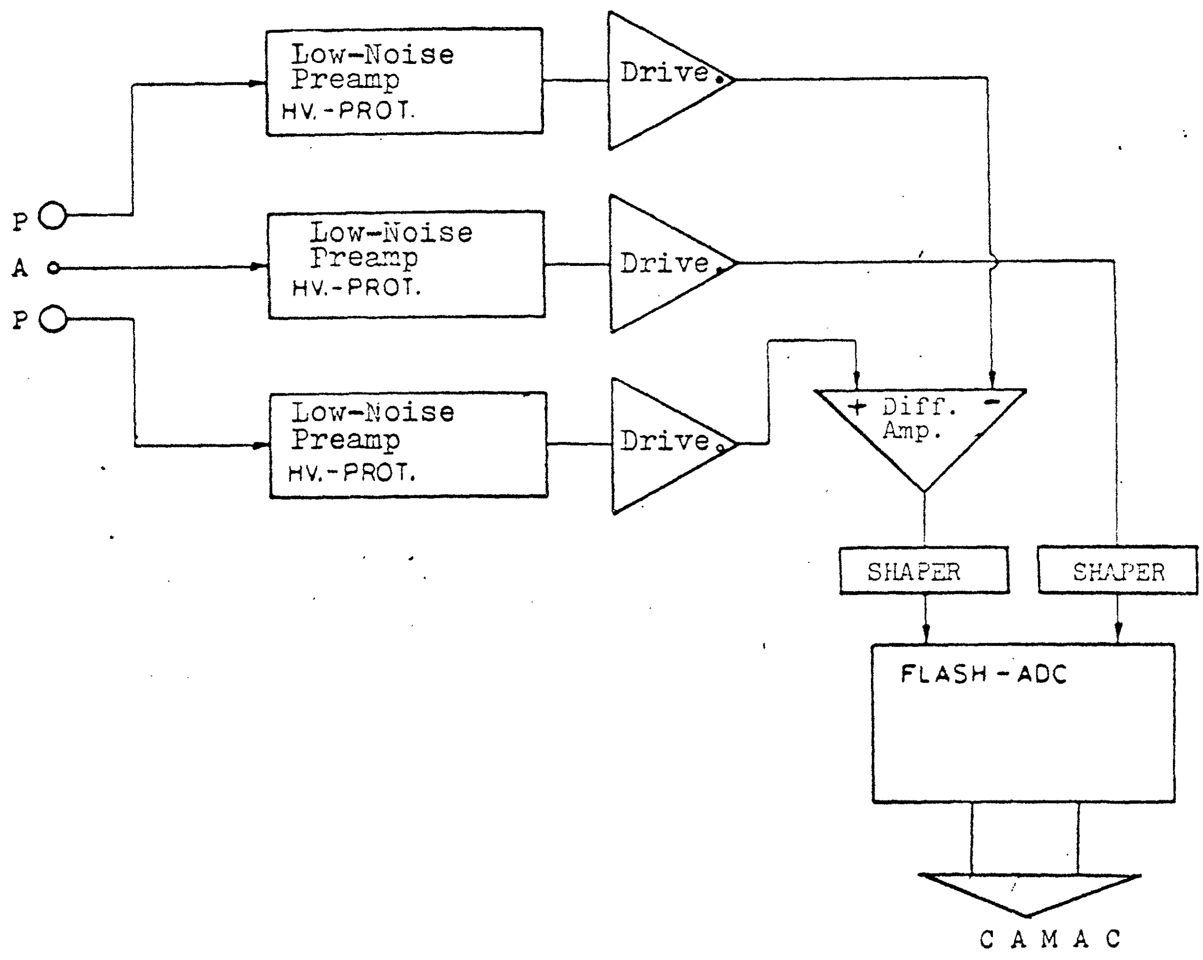
I) Overview

In order to avoid chaos and unnecessary entropy increase, all important information on the TEC analog circuitry has been assembled in this writeup. The "conventional" TEC analog system is diagrammed in Fig. (1) on the following page. Section II) of this report sketches the preamplifier models in current use, and Section III) describes additional circuitry needed to shape and process the signals. Each circuit description contains a brief writeup, schematic, and, if pertinent, print layouts and additional diagrams. Component placement is not indicated on the print layouts; one must use an existing prototype or production model for reference.

Figure 1

ELECTRONICS (ANALOG)

PRECISION WIRE



II) TEC Preamplifiers

All designs in use are based upon a common-emitter-w. feedback first stage (CE-3) amplifier cascaded with a common-base second stage (CB-4). The first-stage is kept inside the gas volume of the test chamber and it drives a 100Ω twisted pair approx. 40 cm. to the exterior of the chamber, series terminated into the second-stage input. The second-stage outputs drive 50Ω cables to the counting room for further manipulation. Design details follow....

II-A) CE-3 Conventional first-stage preamplifier

The schematic (Fig. 2) shows the anode (optimized for negative input signals), and PW (optimized for positive input signals) circuits; identical except for the use of NPN transistors in the former, and PNP in the latter. The output currently drives a 100Ω twisted pair to a CB-4 second stage; if a CB-4 is not used, one must DC isolate the termination resistor from the line via a series capacitor. All transistors are SOT-23 μ-chips. This is an inverting, current-sensitive amplifier.

The printed circuit (Fig. 3) contains one anode and two PW circuits.

Specs.

Rise-time: $\tau_r \approx$ 3. nsec.

Noise: ≈ 2000 e^- RMS over full bandwith

Input Impedance: $Z_{in} \approx$ 140Ω (inc. input resistor)

Power Diss.: P_D = 13 mW/channel

Gain: Anode: 32 dB = 5 mV/μA
PW: 29 dB = 4 mV/μA (Assuming above input impedance)

343 - 18078

Figure 2

FIRST STAGE PREAMPLIFIER

CE 3

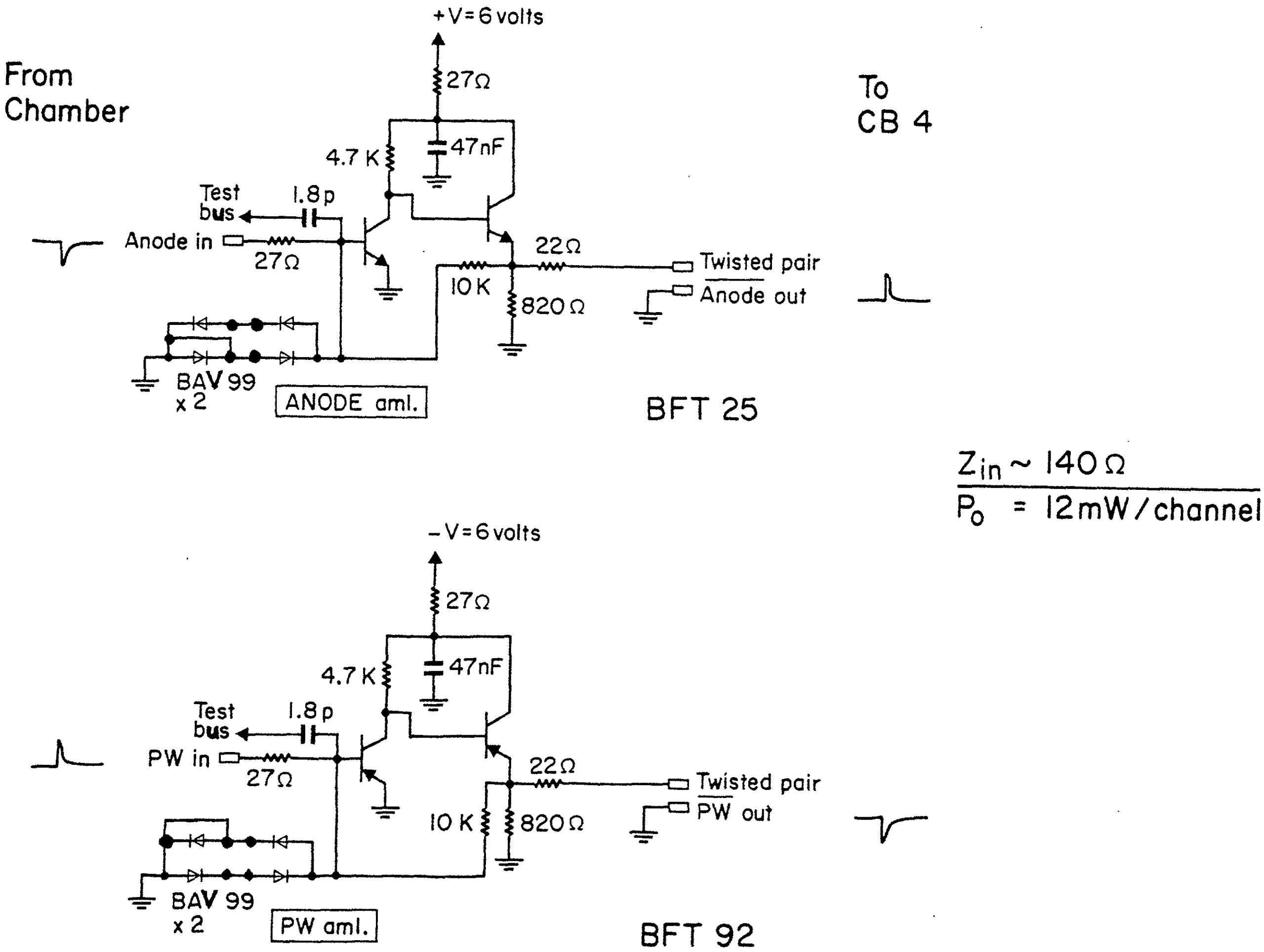
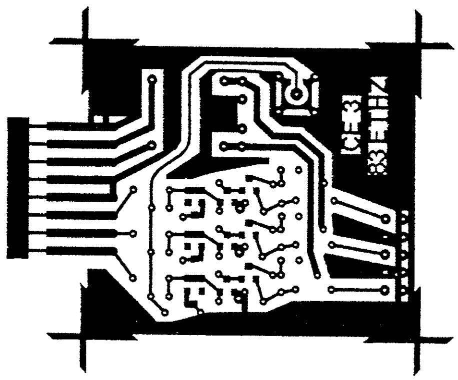
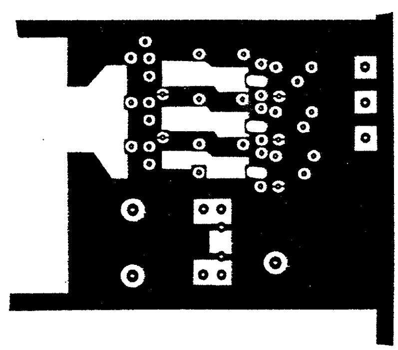


Figure 3



Back side



Component side

POSITIVE

II-B) CB-4 Conventional Second-stage amplifier

The schematic (Fig. 4) shows the anode (optimized for positive input signals) and PW (optimized for negative input signals) designs. The CB-4 is intended to be driven by the CE-3 outputs, and it will drive 50Ω cables.

Note: Each amplifier will drive up to ≳ 2 volts in the optimized direction into 50Ω, however the linearity of the cascade degrades after 500 mV of output (ref. writeup by H. Anders et. al.). The TEC is generally run below this limit, but if larger range is desired, a common-emitter-feedback stage (analagous to the first stage) may be a better choice. One could as well consider using a fast monolithic for the second stage; however until techonology improves further, it is best to keep the head amplifier (which is performance-critical) discrete.

The printed circuit layout (Fig. 5) contains one anode and two PW circuits.

Specs....

Rise-time: $\tau_r \lesssim 3$ nsec.

Input impedance: $Z_{in} \simeq 100\Omega$ (primarily the termination resistor)

Power Diss.: $P_D = 140$ mW/channel

Gain: Anode: 13 dB
PW: 12 dB

Gain of CE-3/CB-4 cascade (2 mV in CE-3, 320 mV out CB-4):
Anode: 44 dB = 22 mV/μA
PW: 40 dB = 15 mV/μA

Figure 4

SECOND STAGE PREAMPLIFIER

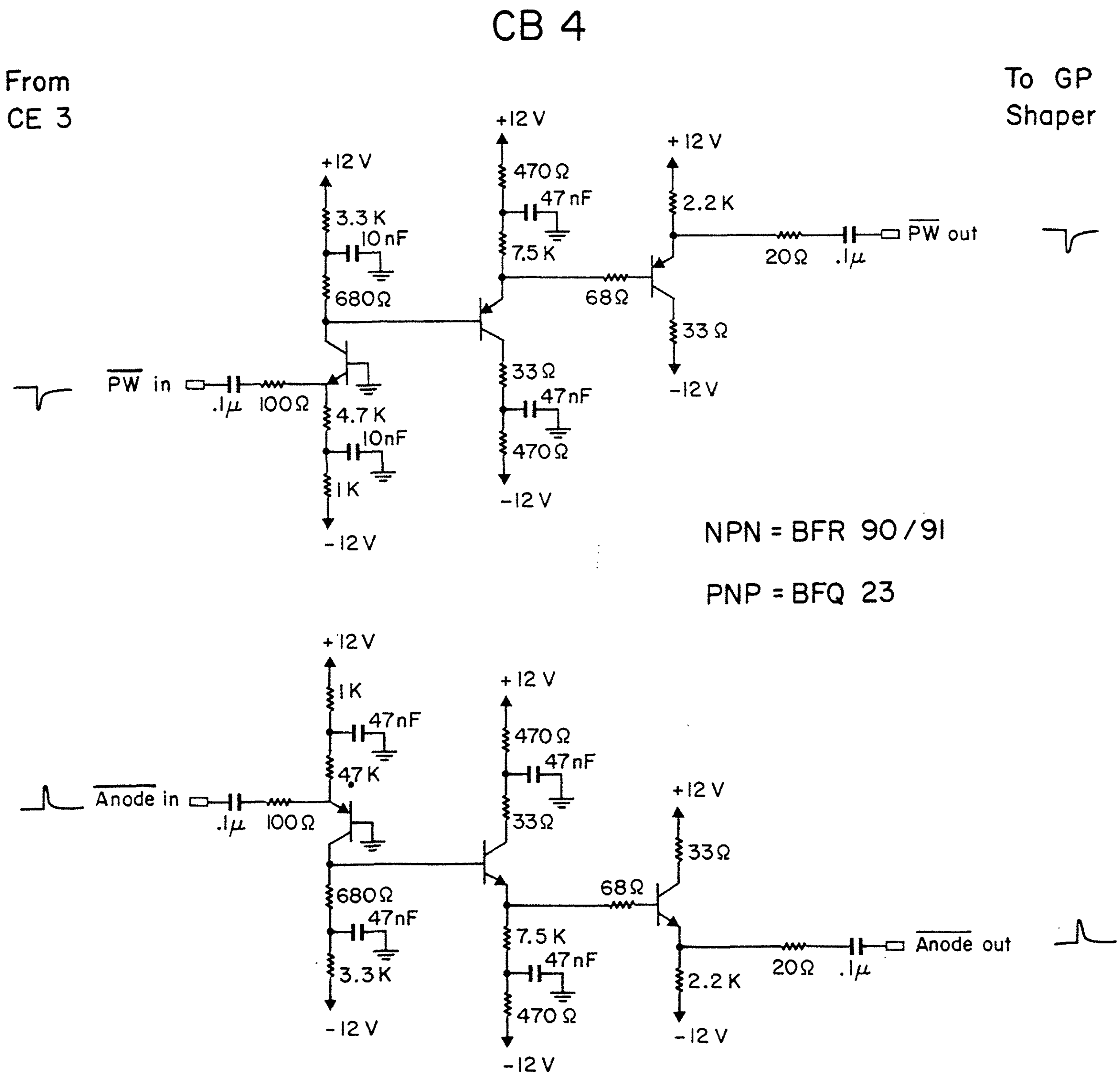
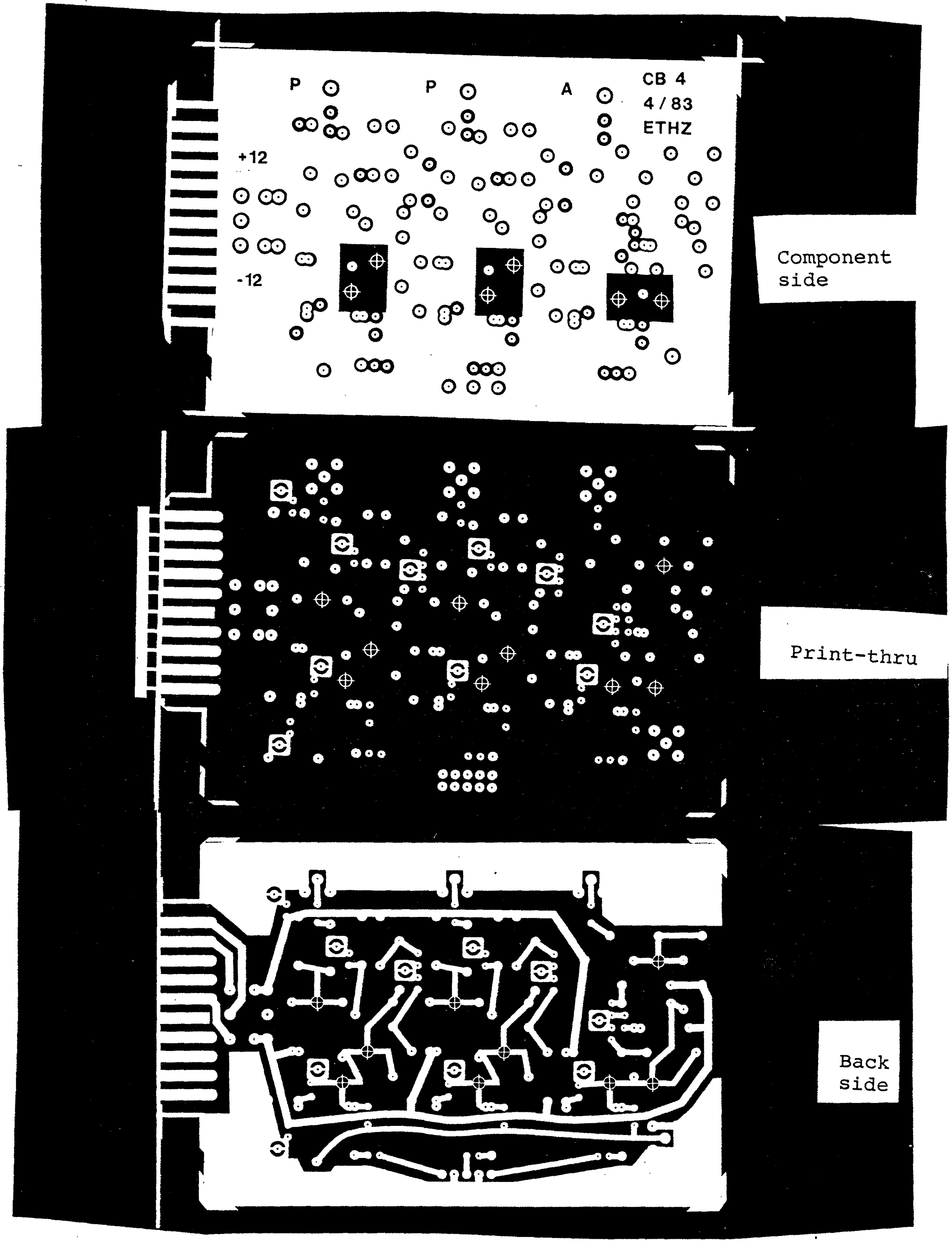


Figure 5



NEGATIVE

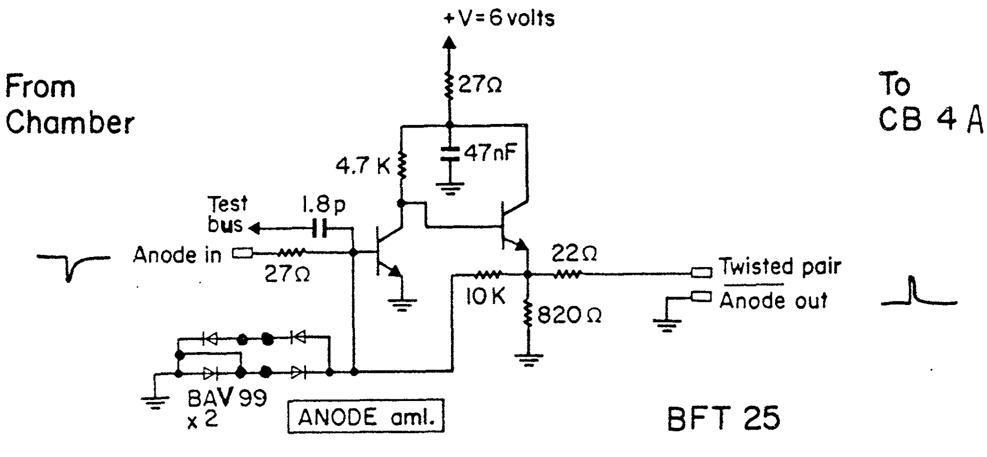
II-C) CE-3A All-anode first-stage preamplifier

As seen in the schematic (Fig. 6), this circuit is identical to the CE-3 design, except for the the print layout (Fig. 7), which contains 3 anode channels (the two PW channels of the CE-3 are replaced). This circuit is intended to drive a CB-4A.

Figure 6

FIRST STAGE PREAMPLIFIER

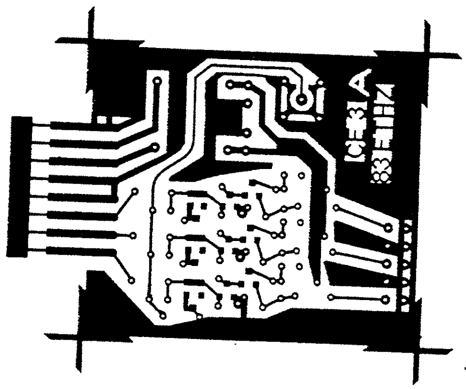
CE 3A



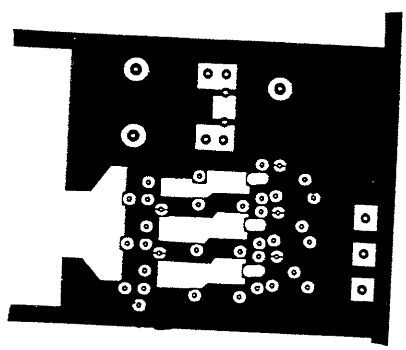
$Z_{in} \sim 140\,\Omega$

$P_0 = 12\,mW/channel$

Figure 7



Back side



Component side

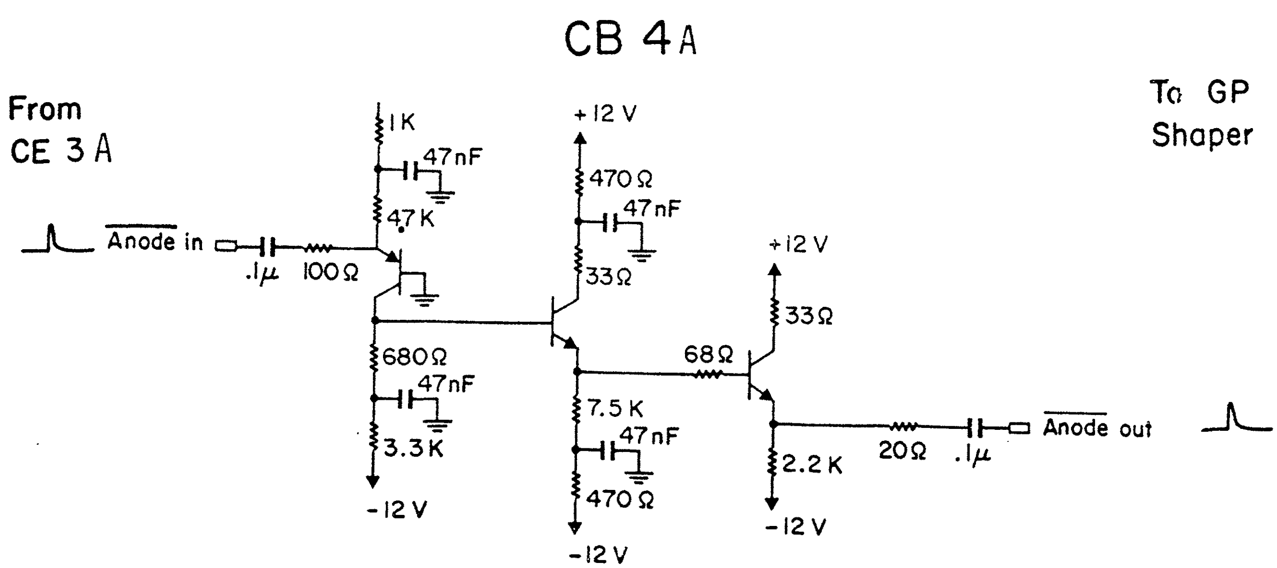
POSITIVE

II-D) CB-4A All-anode second-stage amplifier

As seen in the schematic (Fig. 8), this circuit is identical to the CB-4 design, except for the print layout (Fig. 9), which contains 3 anode channels (the two PW channels of the CB-4 have been replaced). This circuit is intended to be driven by a CE-3A.

Figure 8

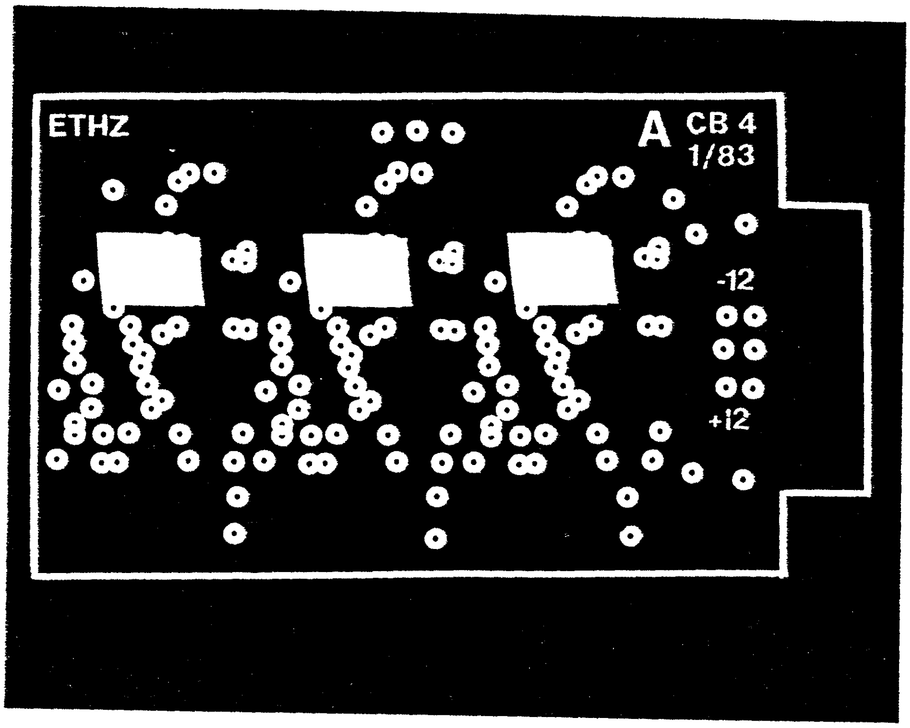
SECOND STAGE PREAMPLIFIER



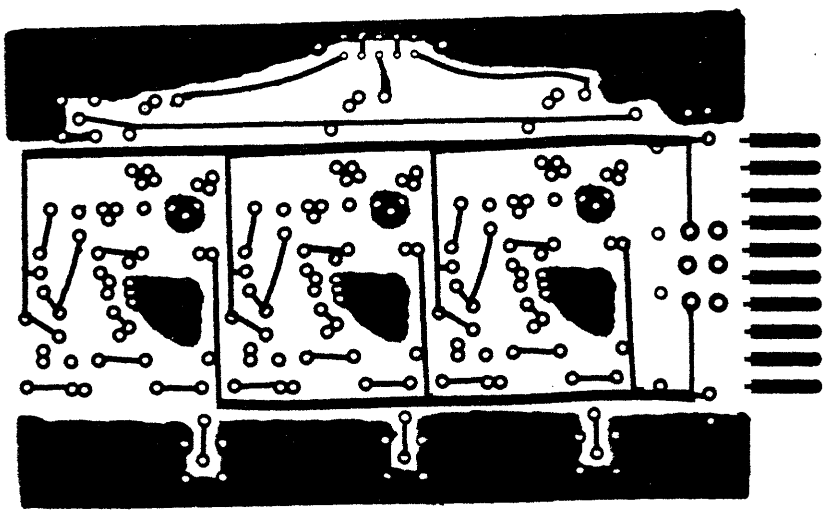
NPN = BFR 90/91

PNP = BFQ 23

Figure 9



Component side



Back side

POSITIVE

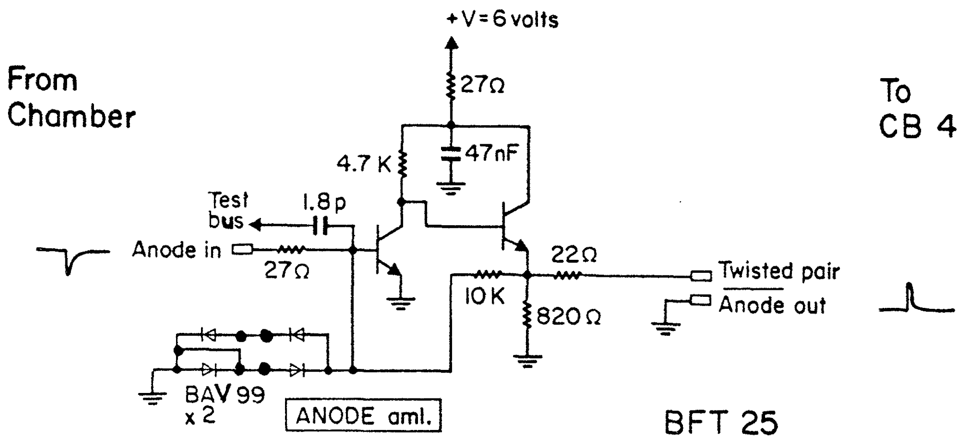
II-E) CE-3P First-stage preamplifier with improved PW protection

In order to better protect the PW channels (which seem prone to destructive breakdown), a modification of the CE-3 pickup channels was made, where an anode-type NPN front-end replaced the PW PNP front-ends (which seemed more breakdown-sensitive). This required an additional PNP transistor per PW channel to buffer the NPN output and drive the negative PW output signals down the 100Ω twisted pair. This transistor, however, raises the quiescent power dissipation of the PW channels to approx. 24 mW/channel. The anode circuit remains unaltered. The schematic is given in Fig.10), but no print layout exists, since the modification was handwired onto the CE-3 boards. Due to better performance of the NPN front-end, this circuit yields about 3 dB more gain in the PW channels over the conventional CE-3.

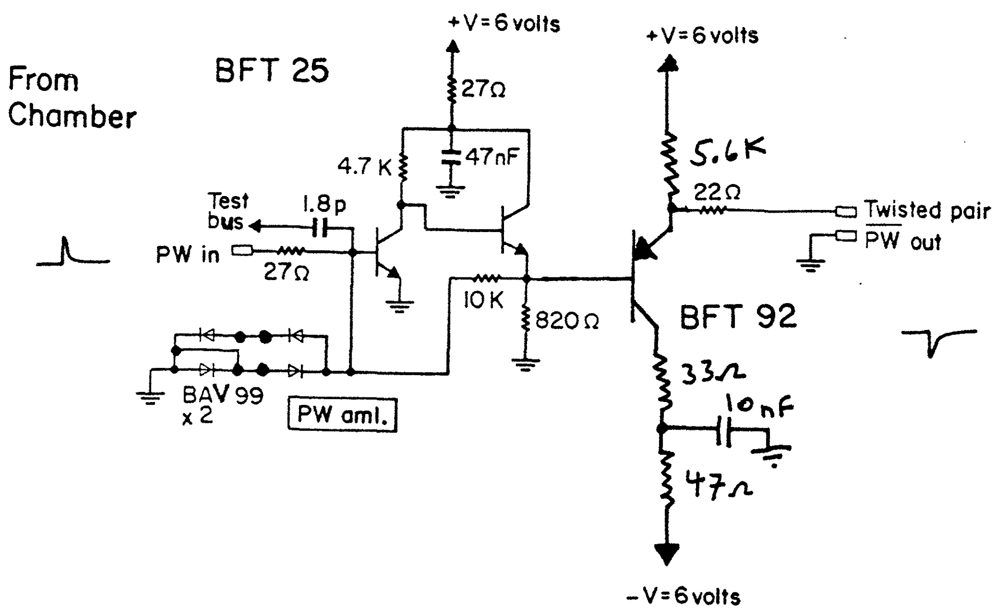
Figure 10

FIRST STAGE PREAMPLIFIER

CE 3P



$Z_{in} \sim 140\,\Omega$



III) OTHER IMPORTANT CIRCUITS

III-A) Differential Amplifier

Fig. 11 is a schematic of the circuit used to subtract the two PW signals. The inverting and non-inverting inputs to A1 are balanced via two trimmer potentiometers (accessable at the front panel). Trimmer capacitor T1 is adjusted to null any overshoot at the amplifier output. The amplifier rise-time is under 10 nsecs., and the "1-2" output will drive up to ±1 volt P-P into a 50Ω load.

Figs. 12 and 13 are the PC layout for a quad NIM module.

Figure 11

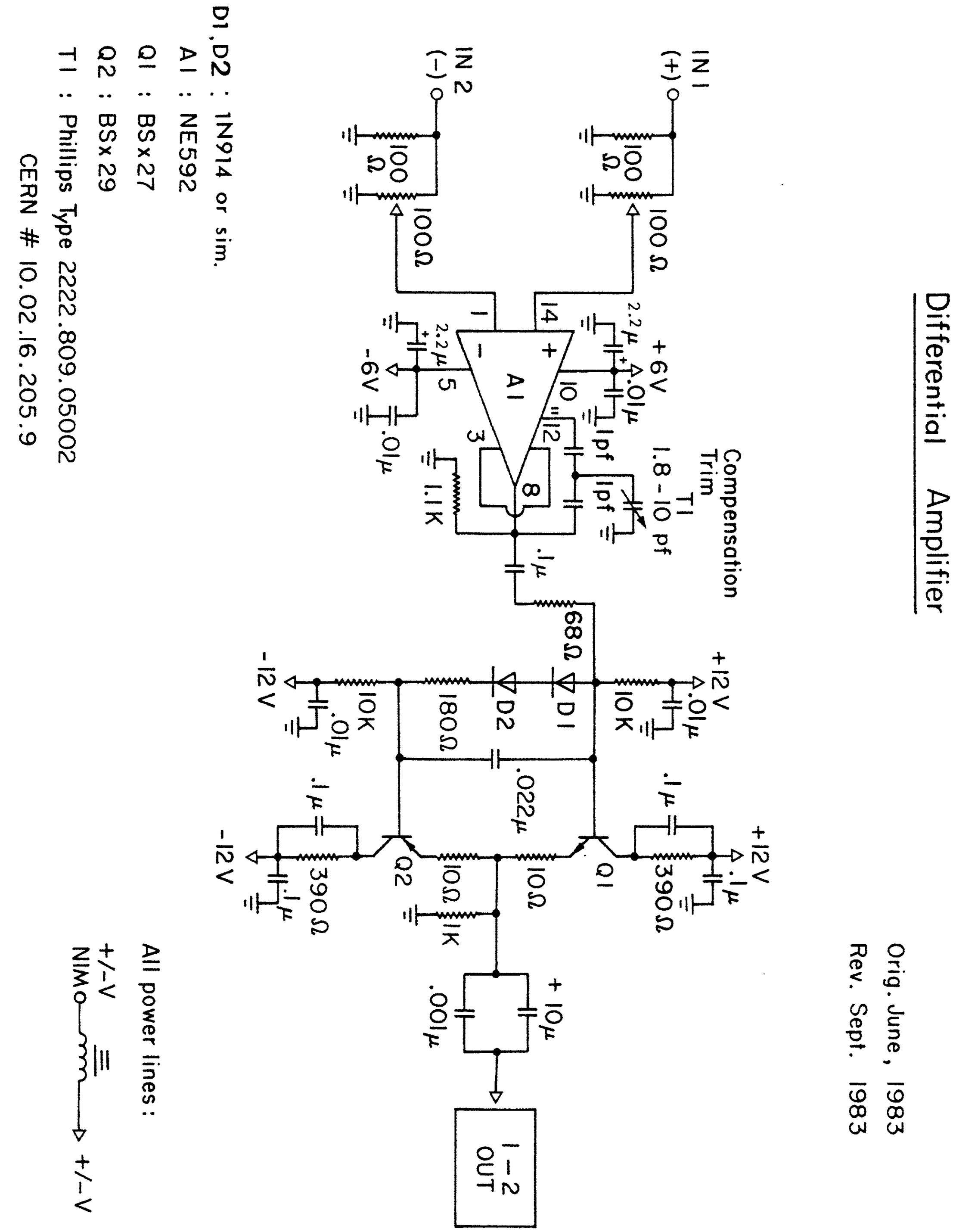
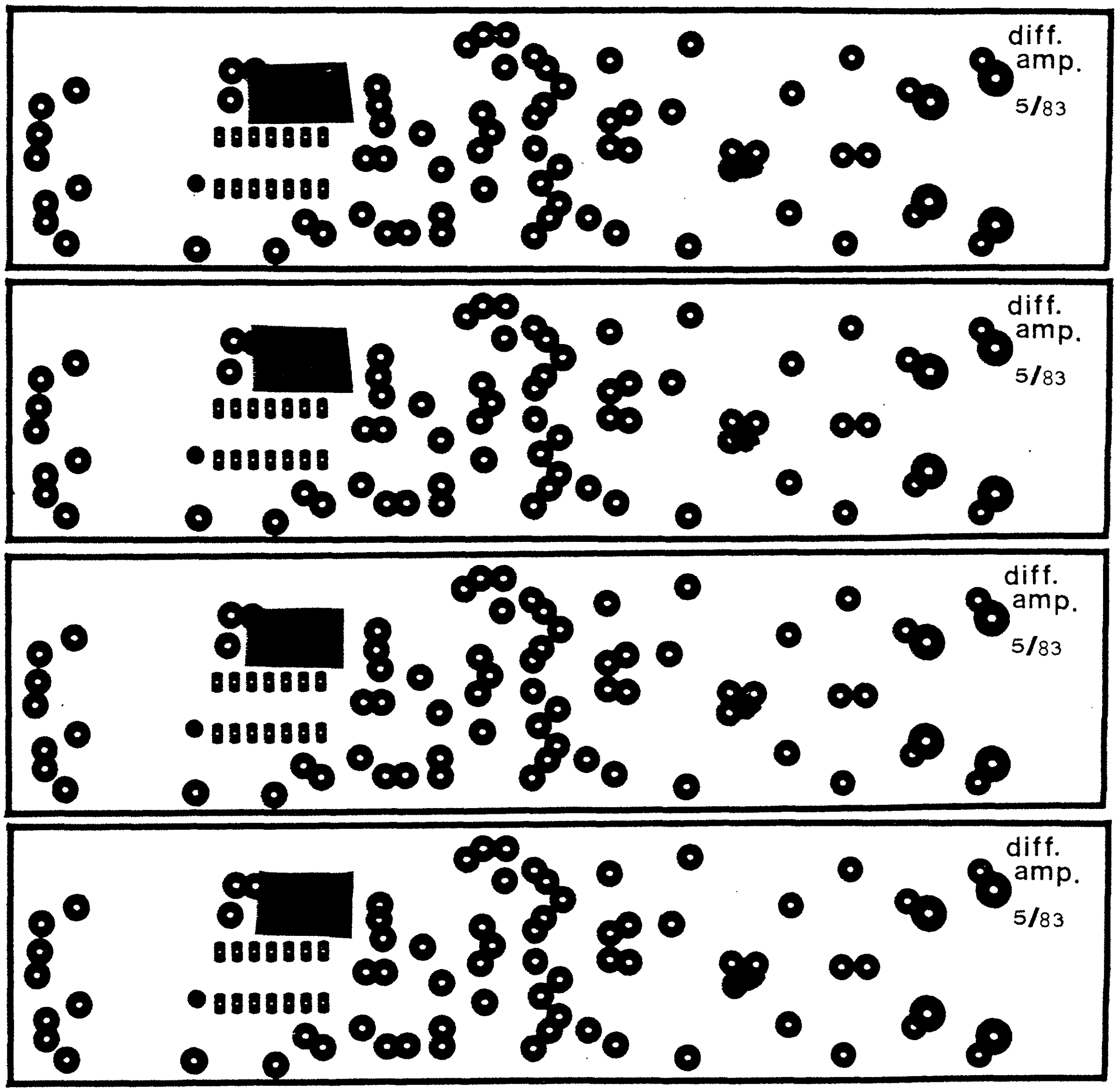

Differential Amplifier
Orig. June, 1983
Rev. Sept. 1983
IN 1
(+)
IN 2
(-)
100 Ω
100Ω
A1
Compensation
Trim
T1
1.8 - 10 pf
1pf
1.1K
68Ω
D1
D2
10K
180Ω
.022μ
Q1
Q2
390Ω
10Ω
1K
+ 10μ
.001μ
1 - 2
OUT
+12V
-12V
+6V
-6V
2.2μ
.01μ
.1μ
All power lines :
+/-V
NIM
+/-V
D1,D2 : 1N914 or sim.
A1 : NE592
Q1 : BSx27
Q2 : BSx29
T1 : Phillips Type 2222.809.05002
CERN # 10.02.16.205.9

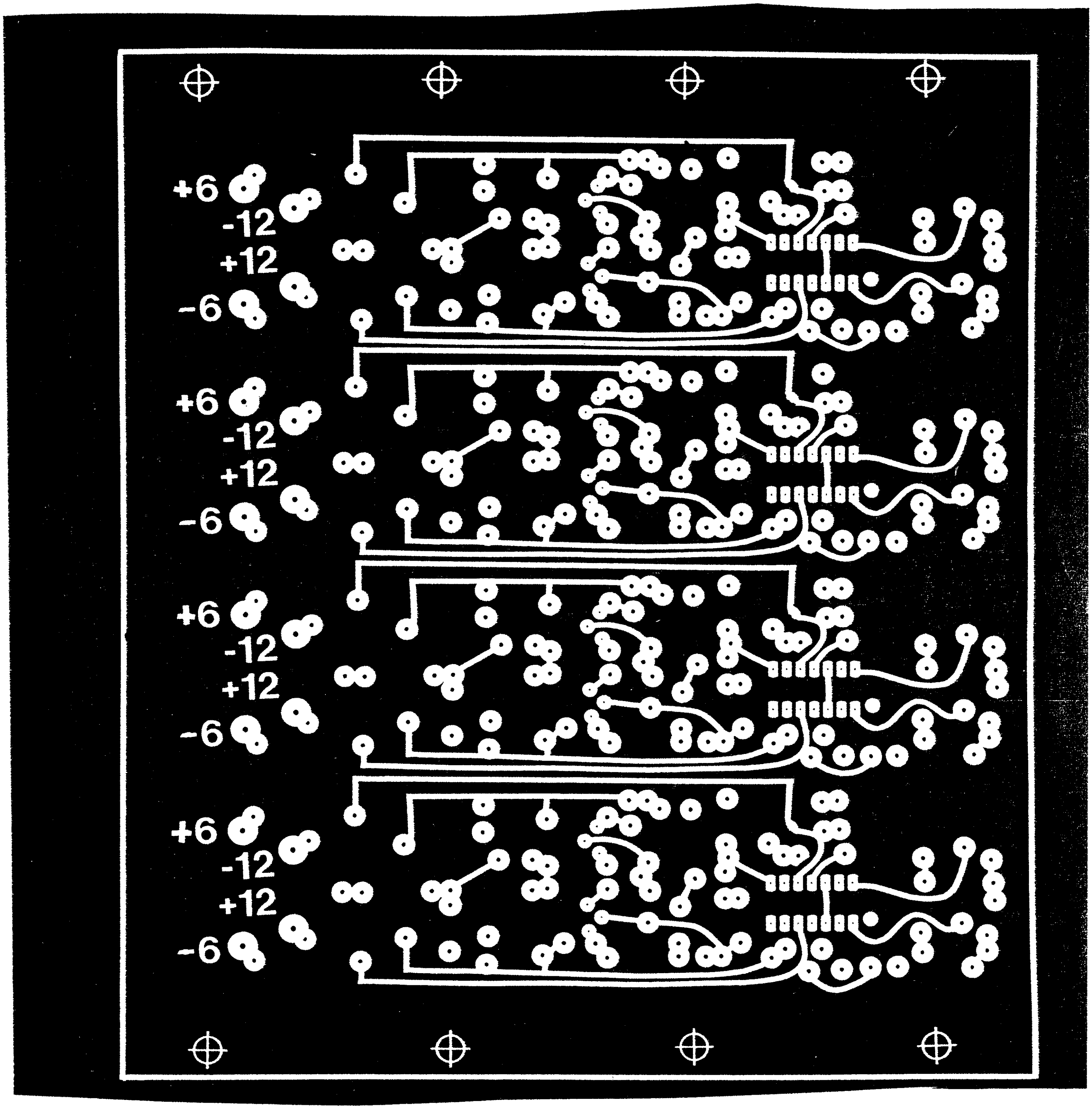
Figure 12



Component side

<u>NEGATIVE</u>

Figure 13



Back side

NEGATIVE

III-B) General Purpose Shaper

Fig. 14 is a block diagram of the circuit used to shape both anode and PWD (Pickup-Wire Difference) signals. The first stage is a pole/zero differentiation (5-10 nsec) which clips the input signal and attenuates any RC tail from the amplifier response. This is followed by a fixed gain stage to restore the signal amplitude, whereupon another pole/zero ($\tau \approx 500$ nsec.) is applied to compensate for the slow ion tail. The signal can then be integrated if desired, and the gain and baseline of the output stage can be adjusted to fit any FADC input requirements. A baseline restorer is in DC feedback around the output stage to compensate for any DC shifts. The schematic is given in Fig. 15.

Fig. 16 shows the location of all shaper adjustments on the printed circuit. The differentiation time-constant (TC) of the first stage is adjusted to the point at which the signal begins to be attenuated; the corresponding pole/zero (PZ) constant is adjusted to remove any undershoot (at the 10-20 nsec. level). The second-stage TC and PZ are then adjusted to remove the slow ($\approx$ 500 nsec.) tail; the TC controls the timing at which the correction has effect (and must be adjusted to "balance" the timing of the signal tail), and the PZ compensates for over/undershoot. There is a slight correlation between first- and second-stage differentiations; the process sketched above should be repeated for optimum shaping.

The integration stage is not currently used (both pots full off {where there is no effect}), but if desired, these pots may be trimmed to "smooth" the signal.

All of the above adjustments should be performed with the gain pot set near minimum. After the signal shape is adjusted, use this pot to bring the signal amplitude up to the desired level.

The DC bias level at the output is adjusted $0 \rightarrow \pm 1$ Volt by the bias pot. The baseline restorer compensation pot should be adjusted to the point at which the shaper output begins to oscillate, and then backed off to a "pinch" after the oscillation ceases. It's always good practice to make this adjustment first (especially if the shaper is oscillating; this is generally why). The hardware strap indicated in Fig. 15 selects a positive or negative bias increment (at present all units are wired positive).

The shaper accepts either polarity input signals up to $\approx$ 300 mV P-P (beware of input stage saturation) and the output will drive over ± 1 volt into a 50Ω load.

The output signal will rise in $\approx$7 nsec.

Figs. 17 and 18 show the PC layout for a quad NIM module.

Figure 14

GENERAL PURPOSE TEC SHAPER

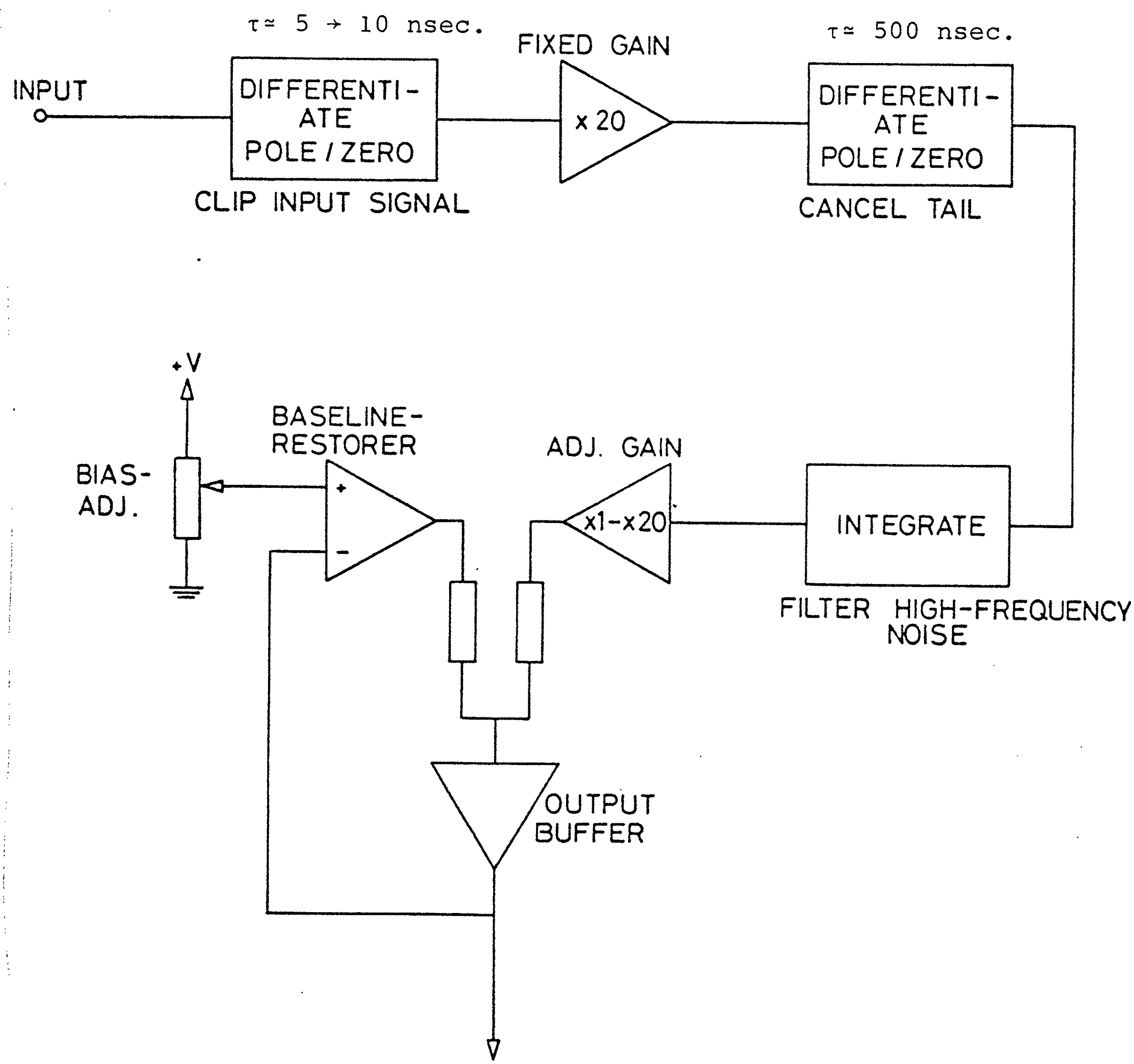


Figure 15

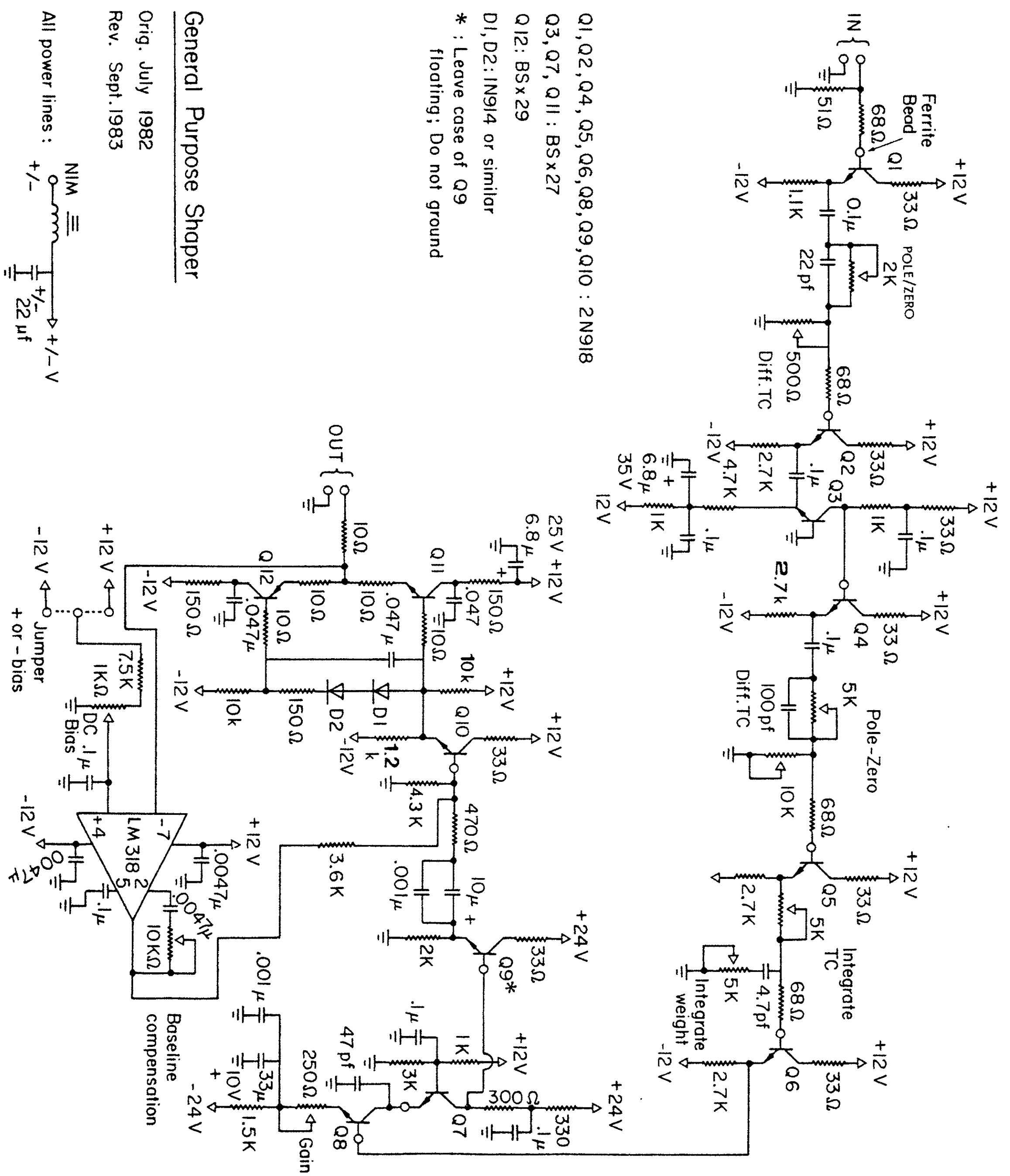

General Purpose Shaper
Orig. July 1982
Rev. Sept. 1983
Q1,Q2,Q4,Q5,Q6,Q8,Q9,Q10 : 2N918
Q3,Q7,Q11 : BSx27
Q12: BSx29
D1,D2: IN914 or similar
* : Leave case of Q9 floating; Do not ground
All power lines :
NIM
+/-
+/- V
22 µf
IN
OUT
Ferrite Bead
POLE/ZERO
Diff. TC
Pole-Zero
Integrate TC
Integrate weight
Baseline compensation
Gain
Jumper
+ or - bias
DC Bias
LM 318

Figure 16

General Purpose Shaper: PC Layout, connections and adjustments

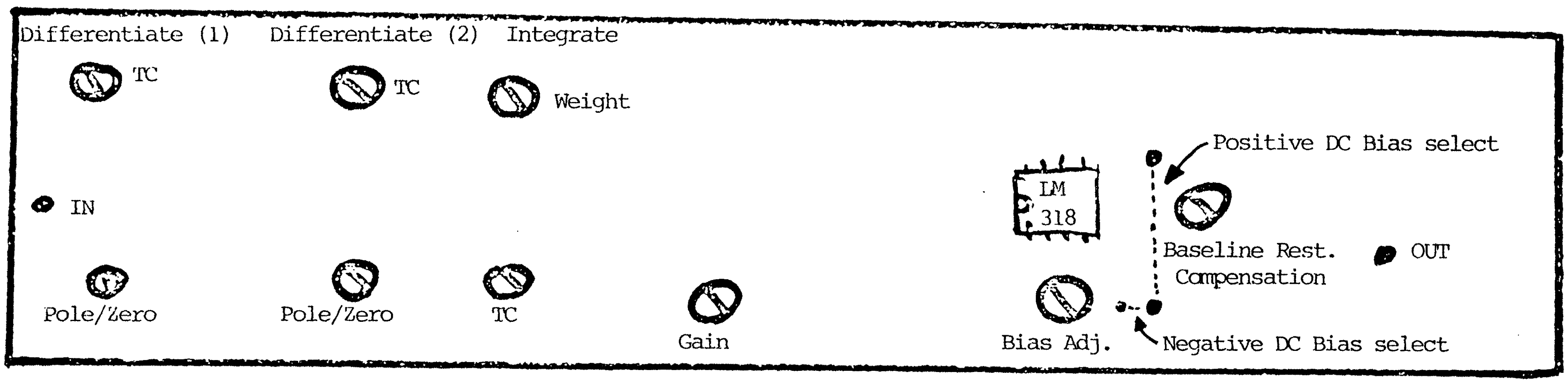
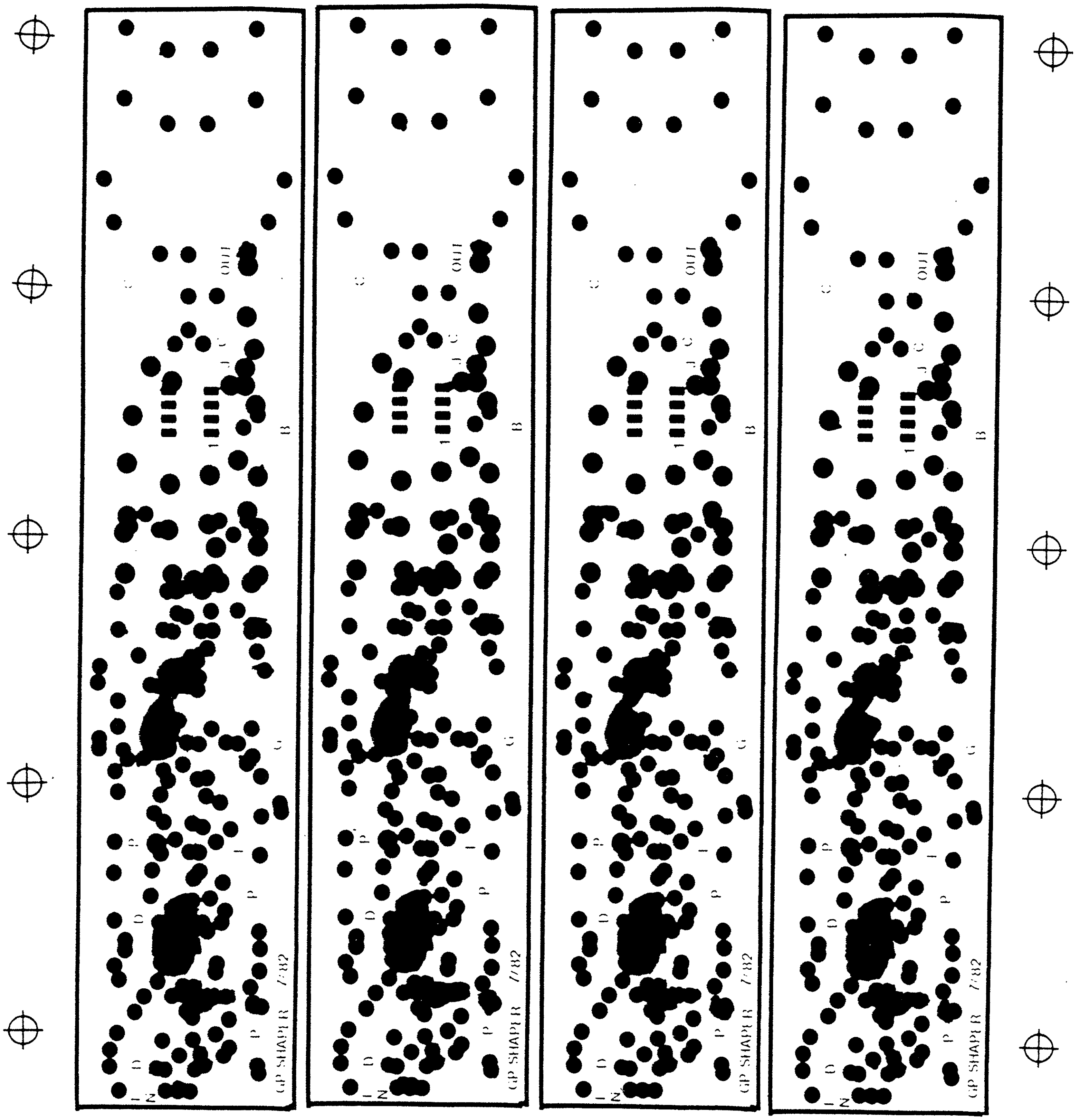


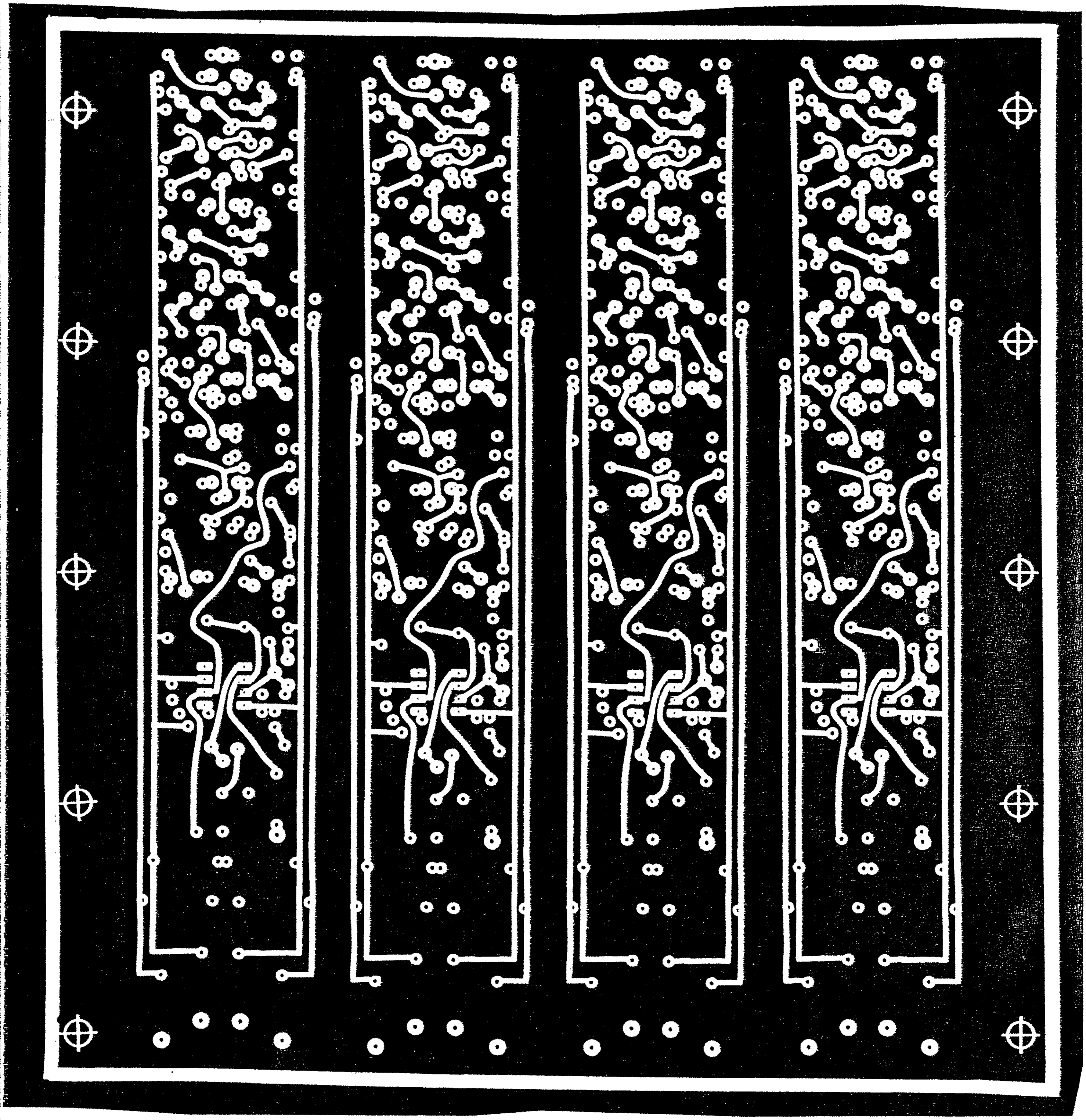
Figure 17



Component side

NEGATIVE

Figure 18



Back side

NEGATIVE

III-C) Fast Positive Fan-Out

Fig. 19 shows the schematic for a circuit which is designed to fan out the second-stage anode amplifier (positive) signals. One such input drives two independent non-inverting outputs and two independent inverting outputs. The outputs will drive over 1 volt into a 50Ω load, and rise in under 3 nsec (non-inverting), and 5 nsec (inverting). The circuit drops ≃ 30% in amplitude between input and outputs.

Figs. 20 and 21 show the PC layouts for a quad NIM module. One very useful feature of this circuit is that the same layout can be used to accept either positive or negative input signals. To accept negative inputs, one need only substitute PNP transistors for NPN's (and vice-versa) and reverse the supply voltages.

Figure 19

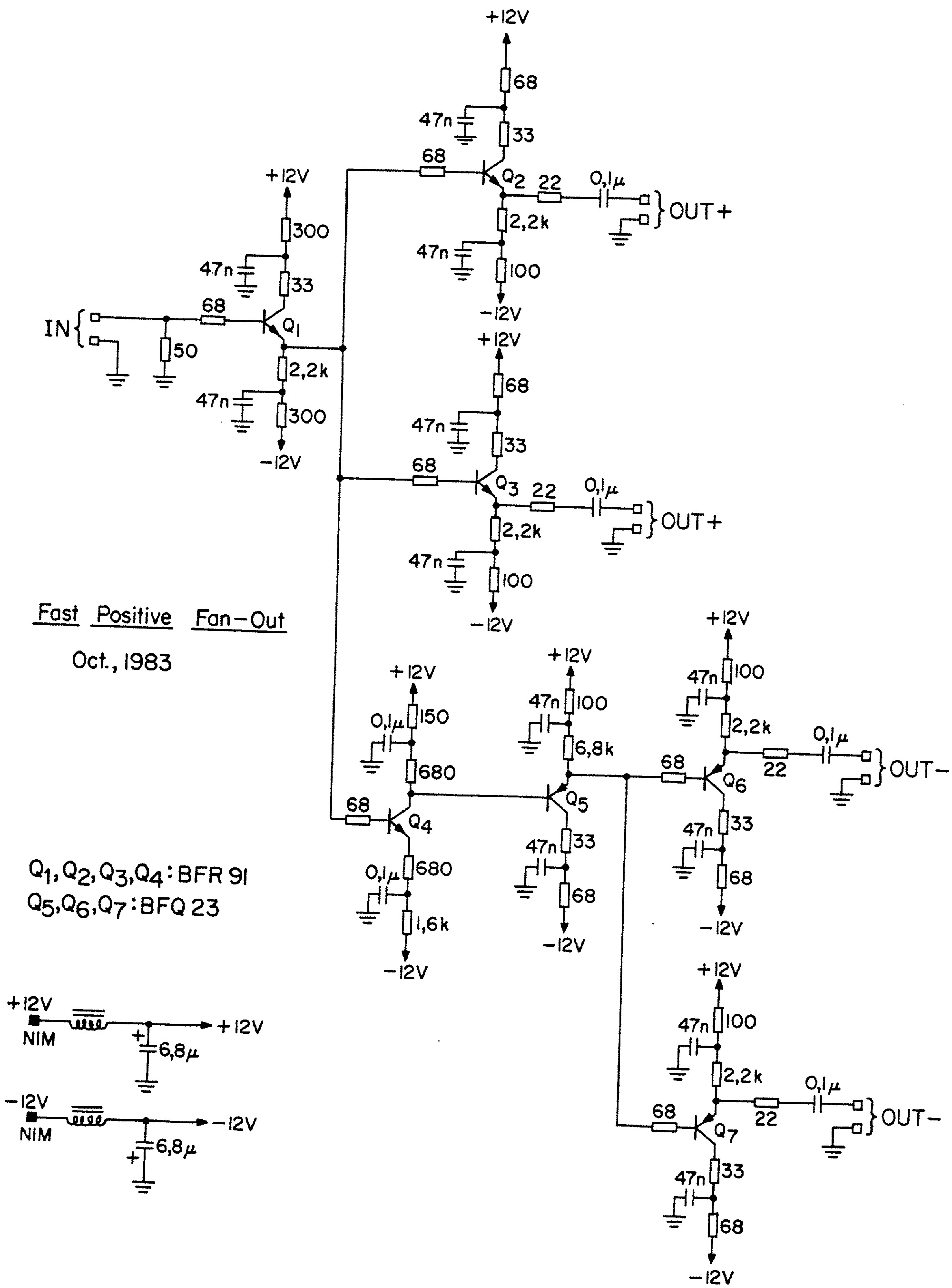
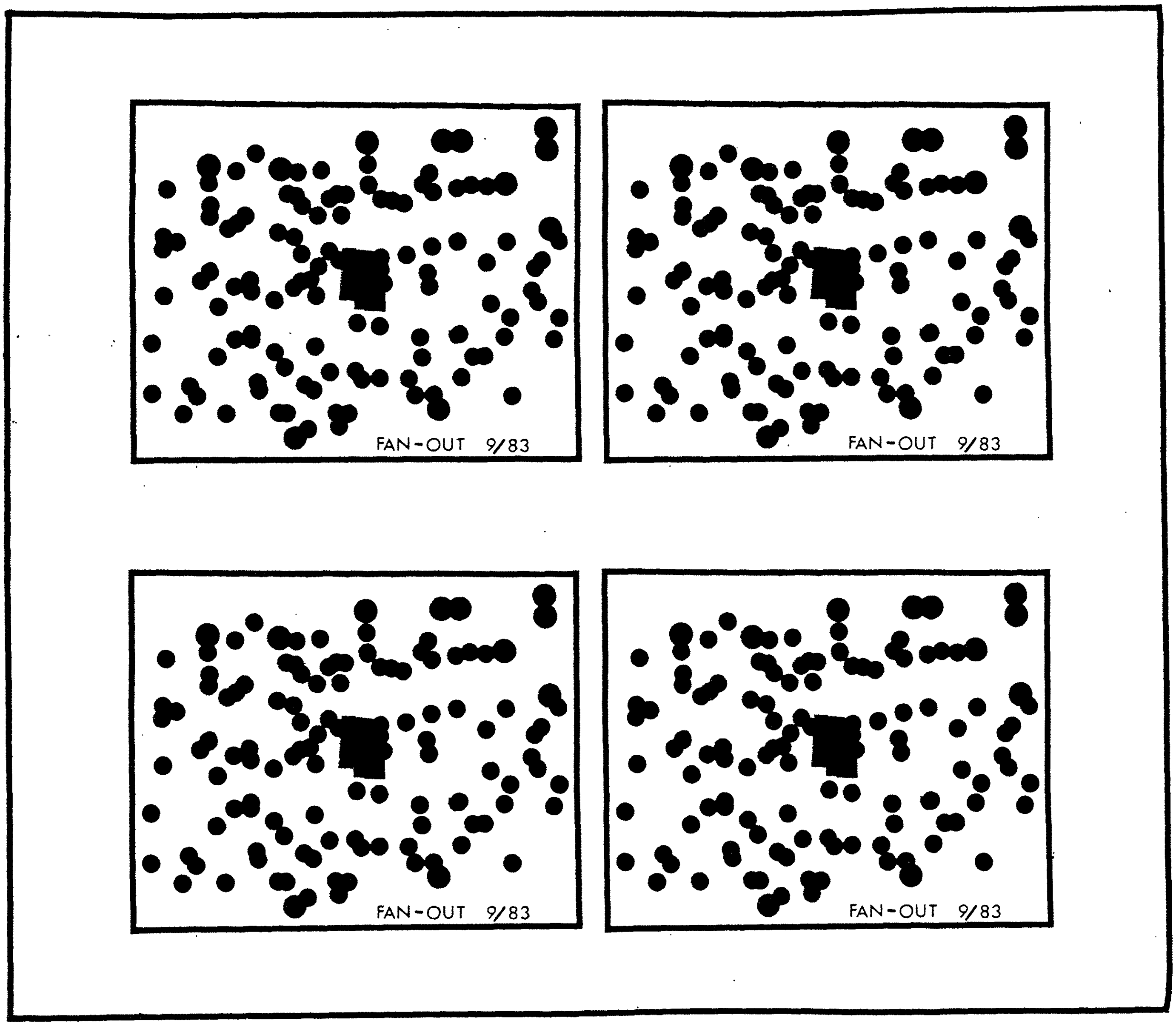

Fast Positive Fan-Out
Oct., 1983
Q1,Q2,Q3,Q4: BFR 91
Q5,Q6,Q7: BFQ 23
IN
OUT+
OUT+
OUT−
OUT−
+12V
−12V
NIM
6,8μ
47n
0,1μ
68
33
22
2,2k
100
300
50
150
680
1,6k
6,8k
Q1
Q2
Q3
Q4
Q5
Q6
Q7

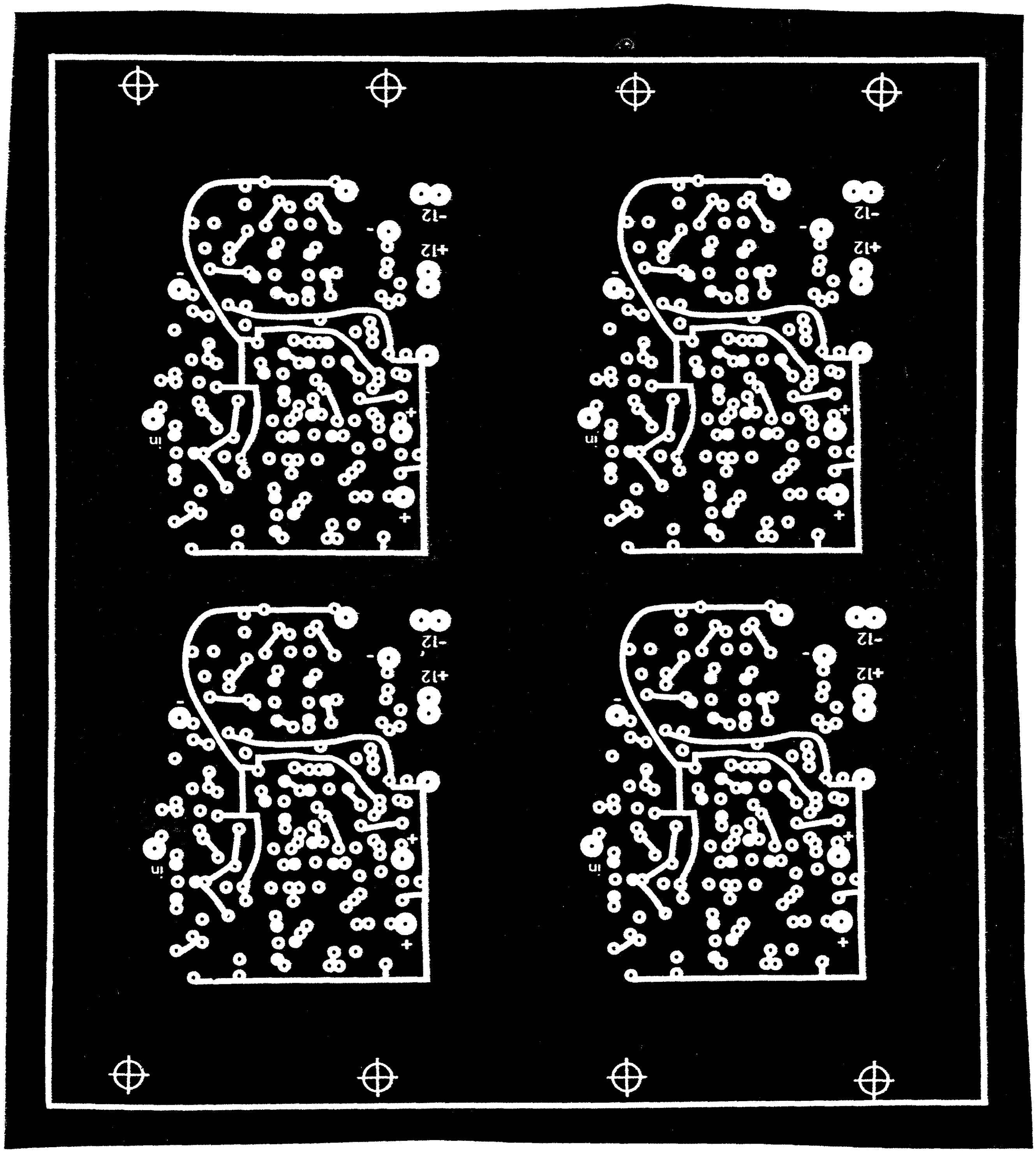
Figure 20



Component side

NEGATIVE

Figure 21



Back side

NEGATIVE

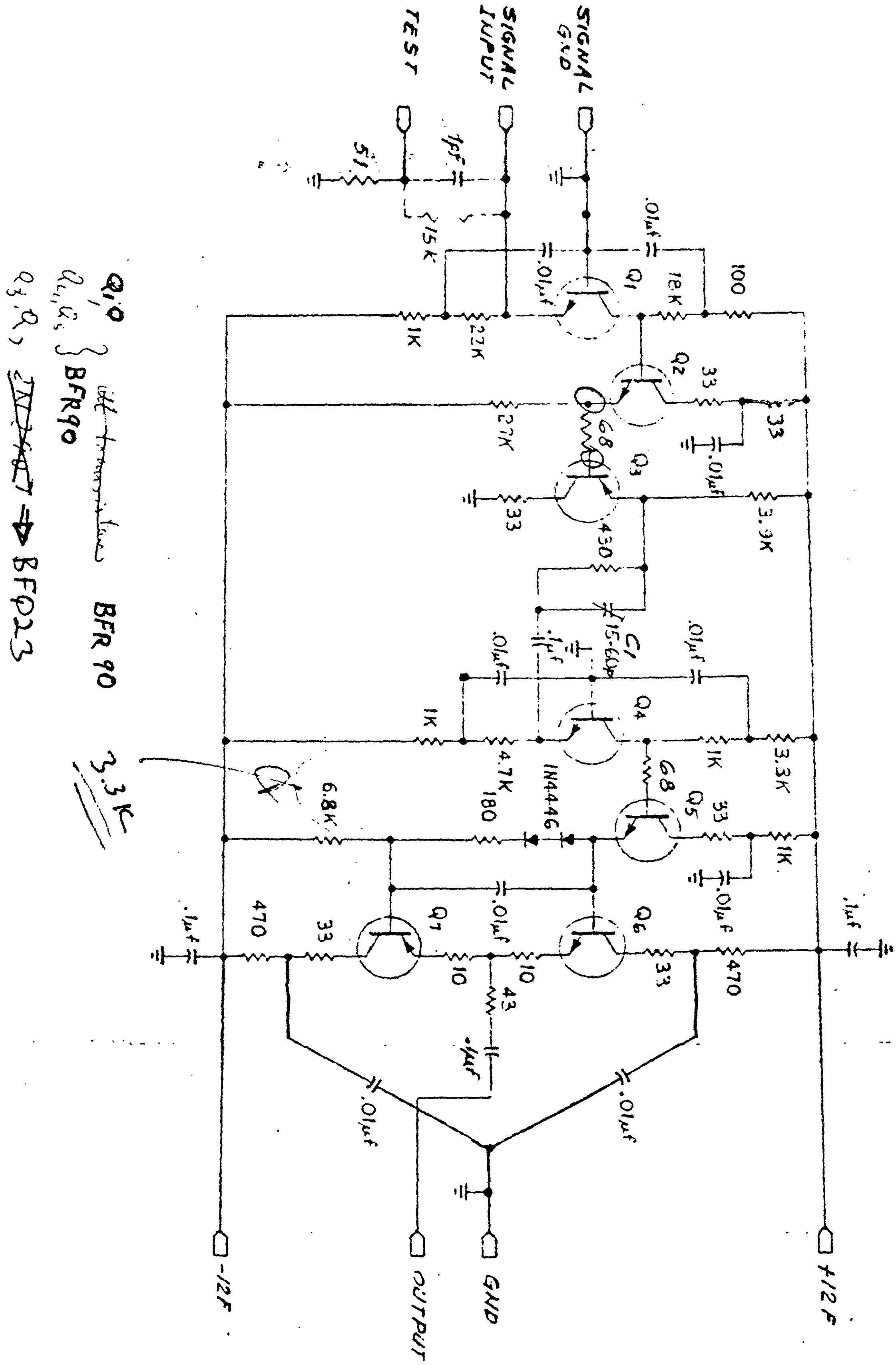
IV) IMPORTED AMPLIFIERS

This section presents 3 amplifier designs developed at BNL which prove puite useful in TEC applications.

IV-A) Common-Base Preamplifier

Fig. 22 shows the schematic and Fig. 23 the layout of a fast 2-stage common-base current-sensitive preamplifier. The CE-3/CB-4 cascade superceeds this for our TEC work (the Pole/Zero correction required between the two common-base stages is a nuisance, especially when they are separated by 50 cm. of twisted pair). The circuit is nonetheless a classic, and is in use by the Hofer group at SIN.

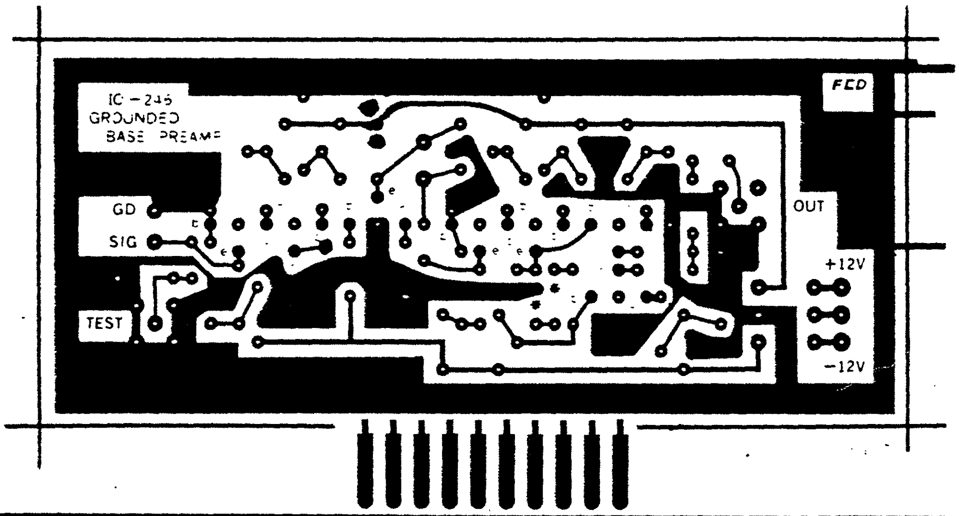
Figure 22

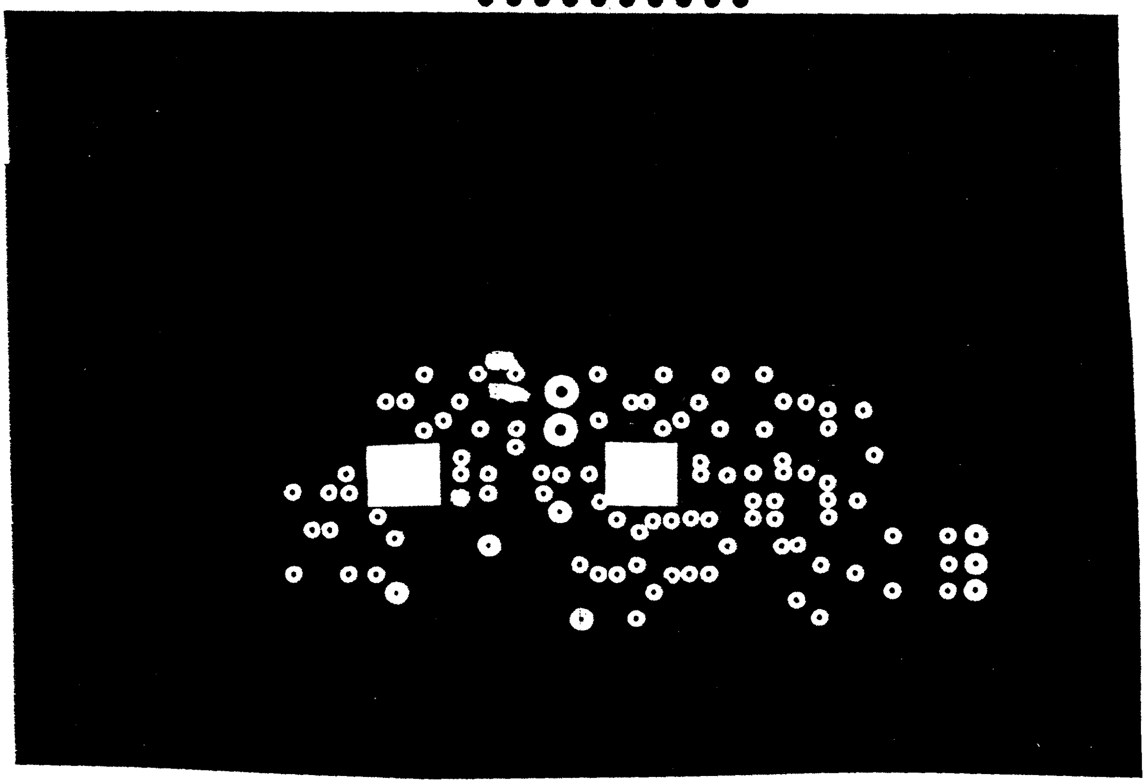


SIGNAL GND
SIGNAL INPUT
TEST
Q1
Q2
Q3
Q4
Q5
Q6
Q7
C1
1N4446
BFR90
BFQ23
3.3K
OUTPUT
GND
+12F
-12F

Figure 23

Back side





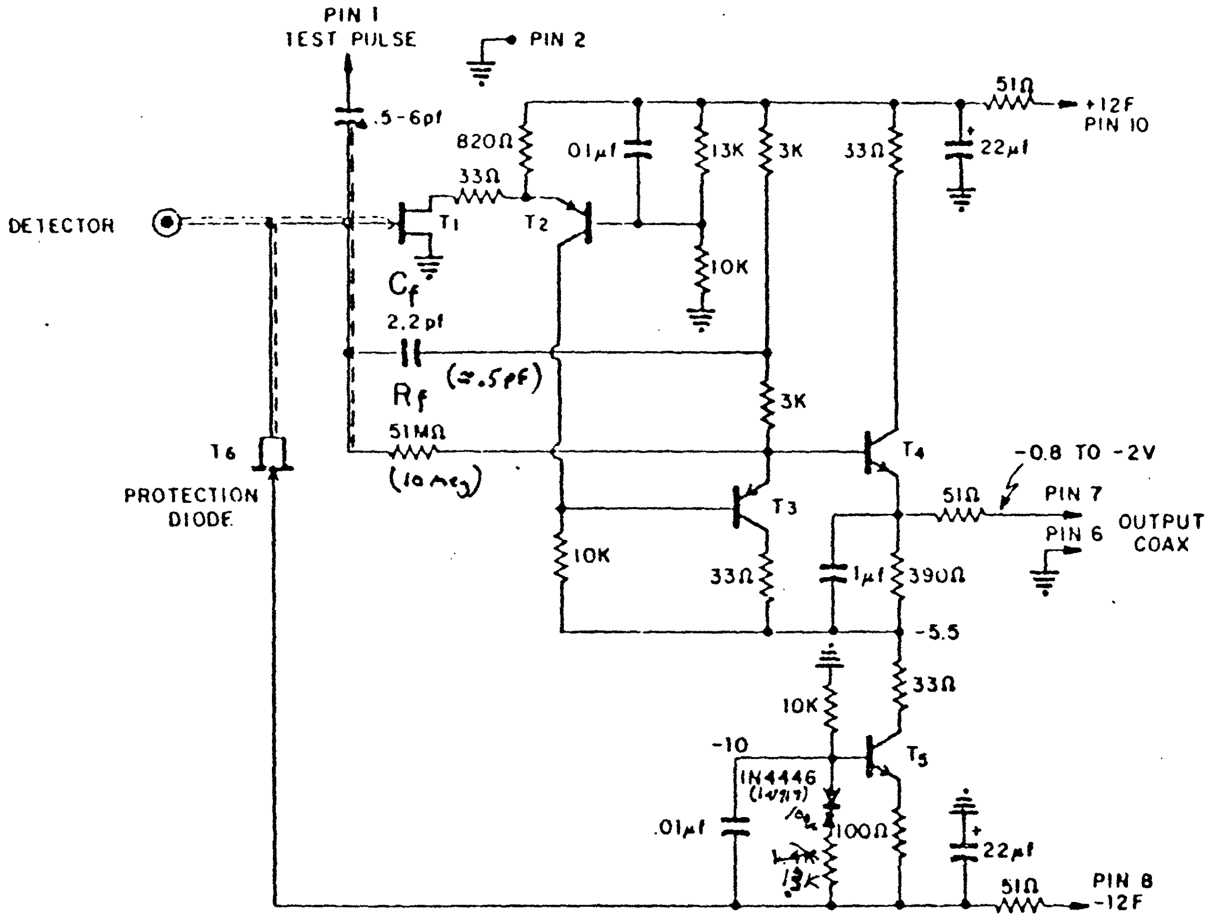
Component side

POSITIVE

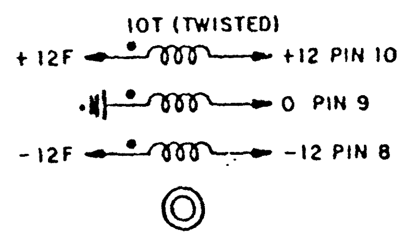
IV-B) Slow Charge-Sensitive Preamplifier

Fig. 24 shows the schematic and Fig.25 the PC layout of a slow (rise-time ≈ 40 nsecs) charge-sensitive amplifier (gain ≈ 6600 e^-/mV). This amplifier <u>is used</u> in our tests to monitor gas gain, thus is quite important. One must beware however; the layouts already prepared at ETH are actually backwards, hence the FET connections are convoluted.

Figure 24

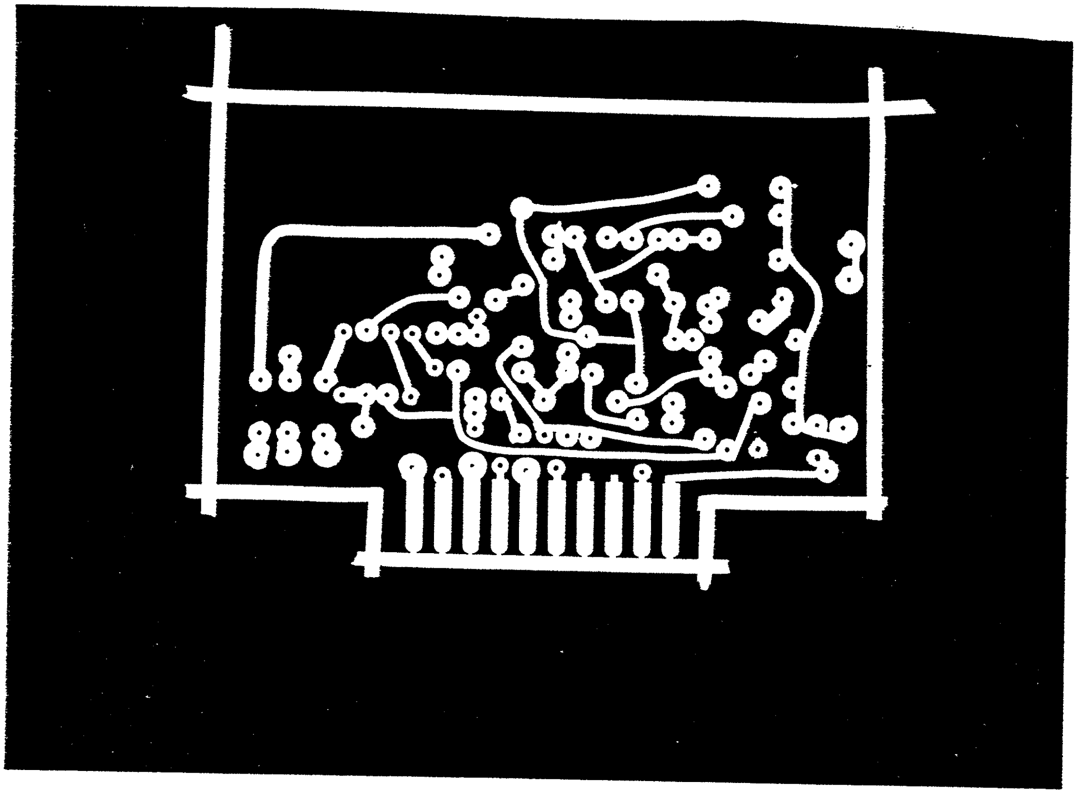


ALL TRANSISTORS IN SOCKETS
T_1 - SFB8558, BF817, 2N4861 (TEXAS INSTR)
$T_{2,3}$ - 2N3906
$T_{4,5}$ - 2N3904
T_6 - 2N4416, OR FAST DIODE WITH $I_r < 10^{-9}$A
DASHED ------
INPUT CONNECTIONS ON TEFLON STANDOFFS AND SOCKETS.

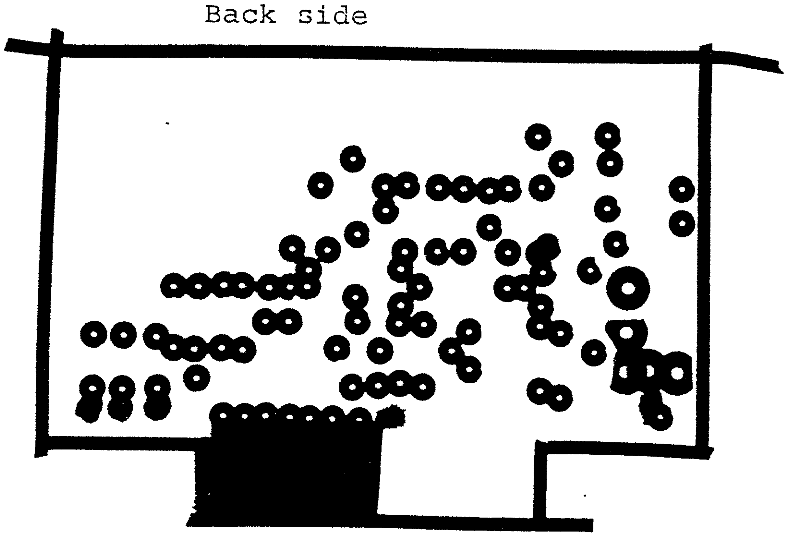


PIN 4 = KEY SLOT
C_0 = 0 FOR WIDEBAND MEASUREMENTS ON LOW CAPACITANCE ION CHAMBERS

Figure 25



Back side



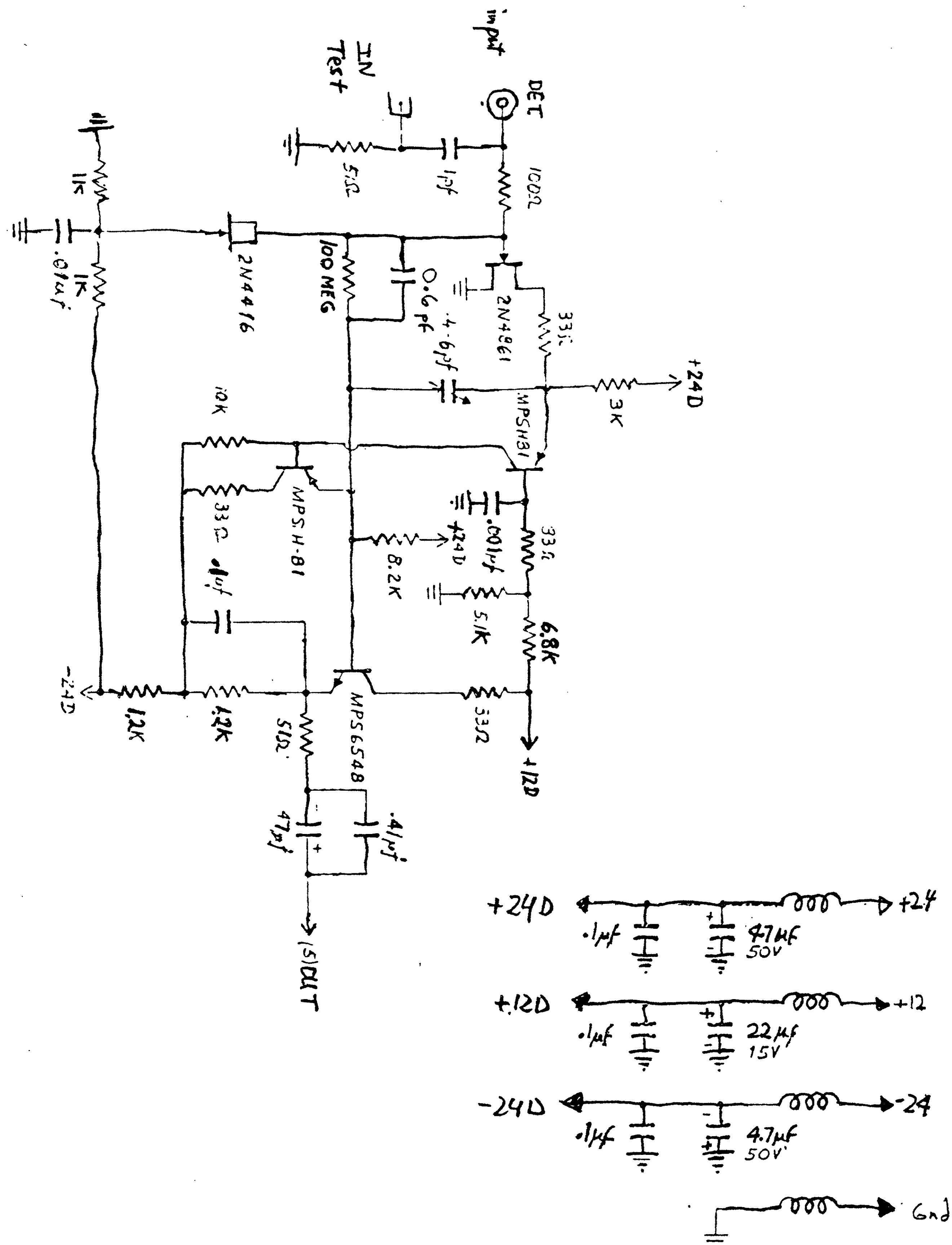
Component side

NEGATIVE

IV-C) Fast Charge-Sensitive Preamplifier

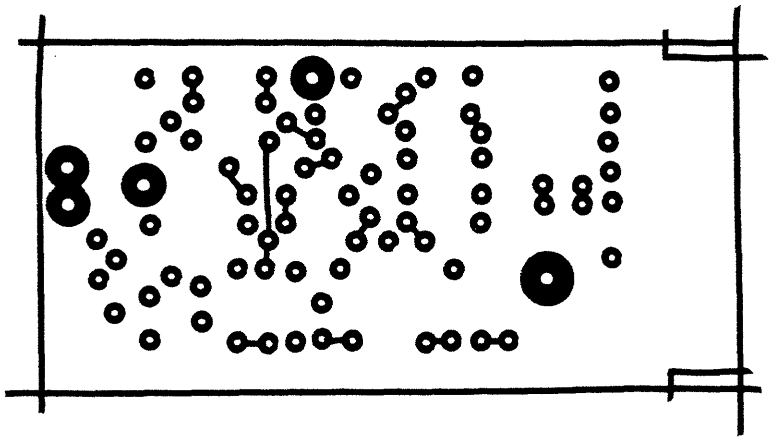
Fig. 26 shows the schematic and Fig. 27 the layout of a faster (rise-time ≈ 8 nsec.) charge-sensitive amplifier (gain ≈ 13000 e^-/mV). This circuit is not currently in use, but is nonetheless quite handy. One must again watch the FET connections (as above), since our prints at ETH seem to be reversed.....

Figure 26

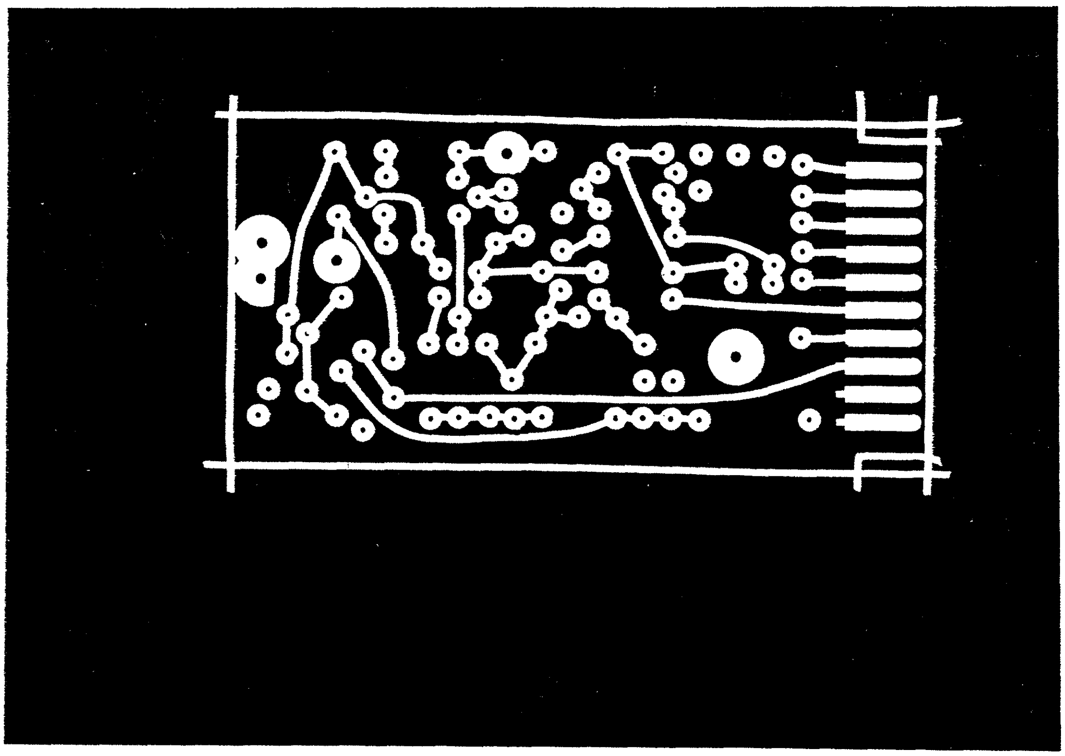


input
IN
Test
DET
100Ω
1pf
51Ω
1K
1K
.01μf
2N4416
100 MEG
0.6 pf
2N4861
33Ω
4-6pf
+24D
3K
MPSH81
10K
33Ω
MPS H-81
8.2K
.001μf
33Ω
5.1K
6.8K
1.2K
1.2K
-24D
51Ω
MPS6548
33Ω
+12D
47μf
.47μf
(51)OUT
+24D
.1μf
47μf
50V
+24
+12D
.1μf
22μf
15V
+12
-24D
.1μf
4.7μf
50V
-24
Gnd

Figure 27



Component side



Back side

NEGATIVE