A Brief Sketch of Proposed TEC Data Flow

The Time-Expansion chamber, as presently defined, consists of an inner cylindrical chamber containing 5 "High Precision" and 4 "Pattern Recognition" wire configurations per sector (12 sectors total) surrounded by an outer cylindrical chamber containing 15 "High Precision" and 14 "Pattern Recognition" configurations per sector (24 sectors total).

Fig. 1) shows the analog signal evolution for each configuration. The precision configuration (Fig. 1A) consists of an anode surrounded by two pickup wires. All three resulting signals are buffered by fast, low-noise, minimal-component preamplifiers located on the chamber endcaps; in addition the pickup signals are subtracted in a fast differential amplifier (commercially available IC such as 733) also located on the chamber endcap. Each precision configuration thus yields two signals (anode + PWD) which are brought out of the "near-end" of the chamber and run to shapers located in an intermediate area (hopefully accessable) approx. 20 meters away. These shapers clip, condition, and amplify the signals, and drive them approx. 35 meters down another set of cables to 100 Mhz, 6-bit FADCS, which are located in the counting-bunker (the front-end of these FADC's will contain an elementary shaper to recover from cable losses).

The pattern-recognition configuration (Fig. 1B) consists primarily of two anode wires which respond independently to tracks traversing either side of the chamber, thus resolving the right/left ambiguity. The Z-coordinate is also derived from this configuration via charge-division, thus both sides of the wires must be read-out. Similar fast, low-noise, etc. preamplifiers as used above buffer the signals, which are subtracted at each end by fast differential amplifiers (733 type as earlier). These are also mounted on the chamber endcaps, and drive 2 cables per configuration (one from near-end and one from far-end) to the intermediate area (the far-end cables consist of thin [roughly 200 um] twisted pairs which will pass between the outer chamber and BGO to the near-end and onward toward the intermed. area), where simple analog units take the sum and difference of these signals, shape them somewhat, and drive the resultants (still two signals) down further cabling to the counting-bunker, where they are digitized by 25 Mhz, 8-bit FADC's. The polarity of the summer output dictates which side of the chamber (right/left) was penetrated by the track, and the ratio difference/sum is the charge-division-derived Z-coordinate.

Total power dissipation on the chamber due to pre-and-difference amplifiers alone will be on the order of 350 Watts.

Every preamplifer channel is equiped with a test pulse input. One test pulse is applied per precision configuration, and two per pattern configuration (one on either side). These come via cable from an addressable pulser. This pulser occupies one crate on each side of the detector (close by), and an address line from the counting-bunker selects the desired channel to test.

In order to facilitate "fine-tuning" of individual wire configurations and to allow for the possibility of disconnecting only one configuration in the case of breakdown or broken wires, it is envisioned to supply each configuration with independent high-voltage lines for the anode and focus wires (in the pattern configuration a third HV line is required to drive a potential wire which is envisioned between the anodes). In addition, we assume two more HV cables per sector (grid and cathode potentials), yielding a total of 2064 HV lines required by the detector. This figure is dominated by the anode, focus, and potential-wire (pattern) channels, which are run at potentials under or around 1 KV, thus bundles of "smaller" HV cables could be used.

Each type of configuration generates two signals which are digitized. Digital signal flow is traced in Fig. 2. The precision-wire signals are digitized into 6-bits at 100 Mhz and dumped into an ECL RAM 1K-words deep.

The pattern-recognition signals are digitized into 8-bits at 25 Mhz and are stored in a conventional RAM 256-words deep. In quiescent operation, the FADC's are continuously clocked (all are driven via a common phase-locked crystal clocking source), and memory is refreshed in a circular fashion. Upon receipt of a STOP signal from the level 1 trigger, the clock is halted and a dedicated firmwired "memory-scan-processor" is started, which reads through the ADC memory and isolates all significant signal "structures" in the data (Note: the scan only inspects one signal per configuration; ie. the anode (precision) or sum (pattern). The other signal is appended when the data is copied into the buffer.). Within approx. 100 usec., this scan is completed for all FADC's, and all such "structure" data (zeroes are skipped) is copied into a buffer which can be read by external "data compactors". An address (prop. to drift time) is affixed to each cell of the FADC data at this point, providing a total of 3 bytes per cell (see tables). A common event number can also be added to the data record here to enable readout synchronization with different parts of the detector. The memory scan processor must monitor the buffer memory limits and provide an "inhibit" signal to the trigger if its buffer is full. If an extrordinarily long signal is digitized (such as when a track curls into a wire), the scan processor can load a coded flag into the buffer and block the massive amount of data generated from being read out. After this 100 usec. scan interval, the FADC clock is restarted, and the front-end system is freed to accept another event. A "veto" signal can be implimented into the scanner, which, upon receipt, halts the scan in progress and restarts the FADC clock. Since the FADC/memory "front-end" is continuously cycling, it requires no "clear" input; if a "stop" signal from the trigger is not received within 10 usec, the memory is automatically overwritten with the immediate signals. All control parameters and thresholds used in the scan processors are downloaded from the host computer.

The phase difference between the STOP signal from the trigger and the next edge of the common clock line yields a timing offset which must be monitored for every event via a dedicated TDC.

The FADC/scan-processor units were envisioned as double-width CAMAC modules in the crates/cost estimate. Because of the large amount of data necessary to transfer and high power dissipation of ECL memory in the 100 Mhz FADC's, a FASTBUS scheme might be more appropriate (in FASTBUS a 2 configuration/slot density might be more appropriate). If a CAMAC-type system is employed, a fast external readout bus is probably required. Data is transferred from the scan processor buffer memories to a set of data compactors over this bus; as much data reduction will be performed in these compactors as time and precision allow; in the worst case (here assumed), the full data record as read from the scan buffers is pushed on toward the host computers and SPI's. See Fig. 2.

A "typical" track traversing the chamber creates signals in 20 precision and 18 pattern configurations. Assuming that a precision signal spans 15 FADC cells and a pattern signal spans 5 FADC cells (at 3 bytes per cell), we have a total of 390 cells per track, yielding one kilobyte per track of zero-suppressed data created. Assuming 30 tracks per event, the acquisition system must handle 30 kilobytes, etc.....

One of the two signals entering the counting bunker per configuration is split and routed to both the FADC (as described) and a simple discriminator, which creates a signal suitable for TDC input into the "early" trigger levels (one must remember the comparatively long drift times [up to 10 usec] in this chamber). The anode of the precision configuration yields one simple discriminated output, while the sum signal from the pattern configuration (which is bipolar) yields two discriminator outputs; one fires when a track is on the left side of the chamber, the other fires when the track is on the right side. See Fig. 1.

Detector monitoring is not elaborated upon in this note; in brief there will be at least three types of data to keep tabs on: 1) peroidic checks on temperature, pressure, mechanical position, high voltages, flow rates, etc. These could be handled by the host mini-computer. A summary of the first four quantities must be occasionally written out to tape for use in the off-line analysis. 2) Laser calibration. This is explicitly performed at the beginning of a run, once or twice per day, or ad infinitum. It creates specific blocks which will probably be saved in the host computer and written on tape. Periodic timing checks can also be performed with the test input on the preamplifiers and addressable pulser. 3) Baseline monitoring. Using zero-suppressed readout in the FADC's is imperative from the point of view of data quantity, but it detracts significantly from information on the signal pedistal. It may be useful to periodically pulse the FADC's and read all of the baselines. This could be handled by the local mini-computer, and summarized data could be passed along to be written on tape.

Based upon 30 Watts power dissipation per configuration for the precision-wire dual FADC/memory-scan-processor unit, and 15 Watts per configuration for the pattern-wire dual FADC/" " (which uses only TTL), we expect about 20 KiloWatts to be dissipated in the counting bunker due to these devices alone.

An additional note on future possibilities is important here. FADC technology is presently in a stage of rapid development, and new design efforts are underway to decrease power requirements (special CMOS techniques, CCD's, phase-shifted clocks, etc.) and increase chip density (more bits, zero-skip logic and buffer memory physically on the chip, etc.). These developments could dramitically drop the large power requirement and meager packing density presently assumed in time for LEP. For reality's sake we have based all of our present assumptions upon today's capabilities and our present experience, but new developments such as outlined above will be followed closely and should be kept in consideration.

-- J. Paradiso 29-April-1983

The following table contains a summary of a few pseudo-quantitative details:

STATISTICS:

# of precision configurations / sector (inner):	5
" "/ sector (outer):	15
" " in vertex detector:	420
" " hit per track:	20
# of pattern configutations / sector (inner):	4
"/sector (outer):	14
" in detector:	384
" hit per track:	18
# of cables detector to intermed. area (precision):	2 x 240 = 340
" " (pattern):	2 x 384 = 768
# of cables intermed. area to bunker (precision):	2 x 420 = 840
" " (pattern):	2 x 384 = 768
# of cables far-end to near-end of chamber:	384/2 = 192
# of cables (total) test pulse distrib. to preamps:	2 x 384 + 420 = 1188
# of HV cables needed per sector (inner):	2 + 2x5 + 3x4 = 24
"(outer):	2 + 2x15 + 3x14 = 74
Total # of HV cables needed in detector:	12x24 + 24x74 =2064
Power dissipation on detector per precision config.:	250 mW
Power dissipation on detector per pattern config.:	530 mW
Power dissipation on detector (endcaps) due to preamps:	350 Watts
Power dissipation in bunker (FADCs) per prec. config.:	30 Watts
Power dissipation in bunker (FADCs) per pattern config.:	15 Watts
Total power dissipation in bunker (due to FADC units):	20 kWatts
# of CAMAC-type slots per config. (FADC):	2
Total # of CAMAC-type crates required (FADC):	75
Power dissiaption in intermed. area:	1 to 3 kWatts
# of equipment racks needed in intermed. area:	6 (approx.)

NOTE: Some additional cabling and hardware is required for low-voltage transport (preamps), laser calibration, and position, temperature, and pressure monitoring. This is not accounted for here. No additional Z-detection scheme (strips, tubes...) is considered in these estimates.

Data Format (output from memory scan processor):

Precision:	I ANODE I	PWD I	ADDRESS	I--I
	6-bits	6-bits	10-bits	2-bits (spare)

Pattern:	I SUM I	DIFF. I	ADDRESS I
	8-bits	8-bits	8-bits

# of bytes per FADC cell for precision configuration:	3
" " pattern configuration:	3
# of FADC cells (avg.) per precision signal:	15
" " pattern signal:	5
# of FADC cells created (avg.) per track:	390
# of bytes created (avg.) per track:	3 x 390 = 1k

Timing.....

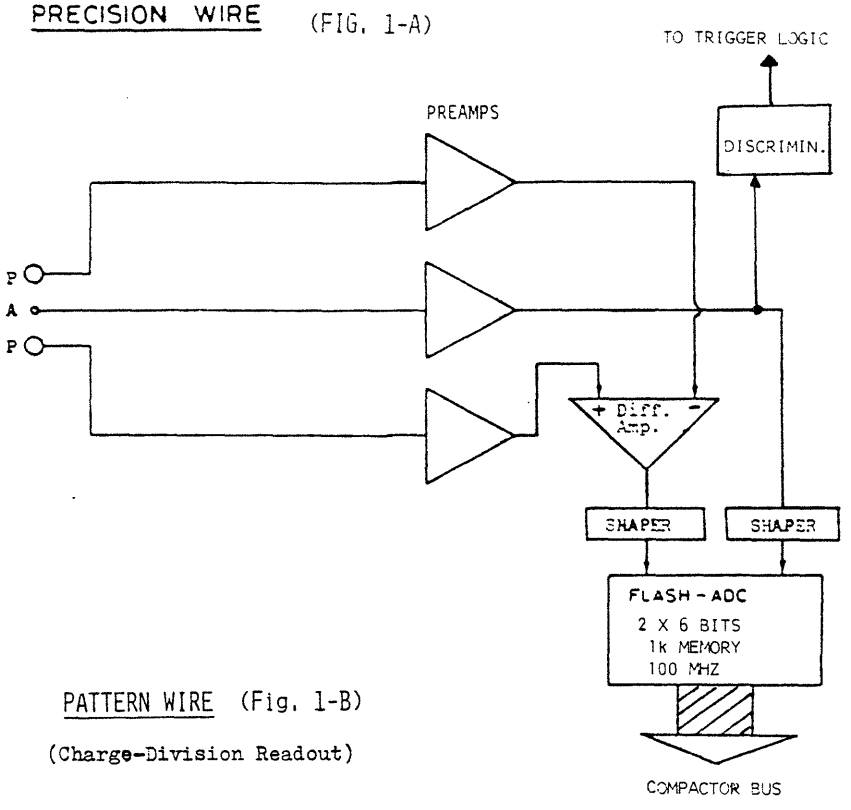
Maximum drift time in chamber:	10 usec.

[NOTE: This depends on drift velocity; here we have assumed that the drift velocity is adjusted such that the outermost wire exploits the full 1k memory depth at a clocking rate of 100 Mhz in the FADC units. This yields a drift velocity on the order of 6 um/nsec.

Maximum time required by scan processor:	100 usec.
Time required to transfer data through compactors:	probably msec. level

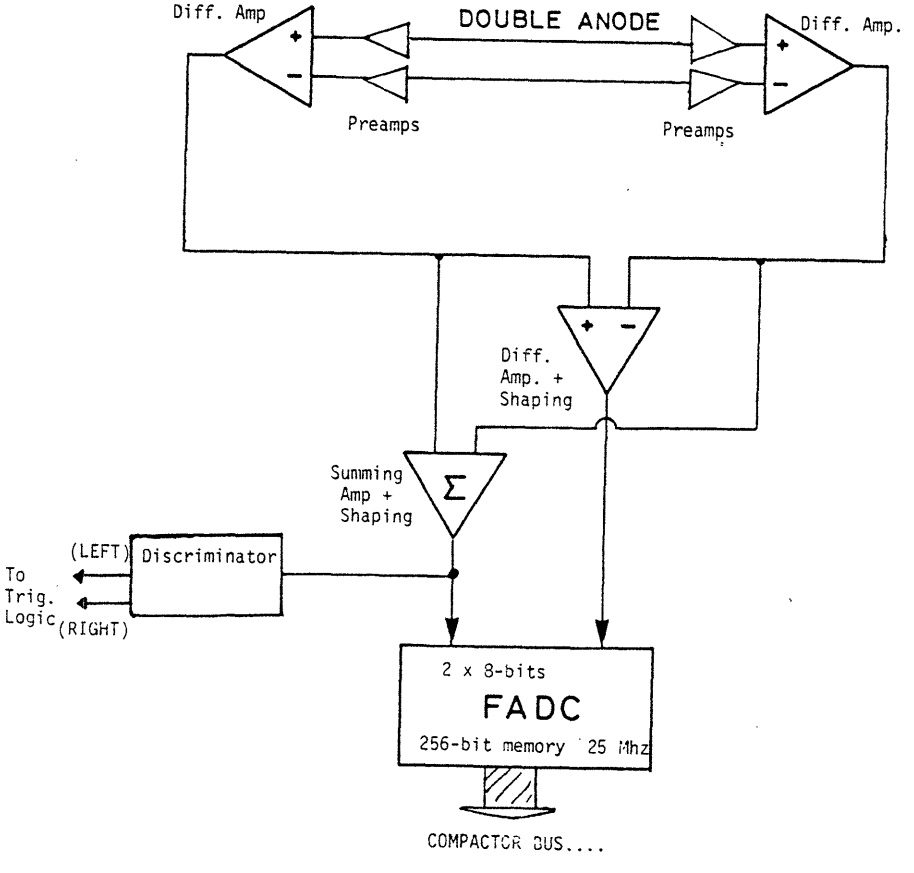
ELECTRONICS (ANALOG)

PRECISION WIRE (FIG. 1-A)

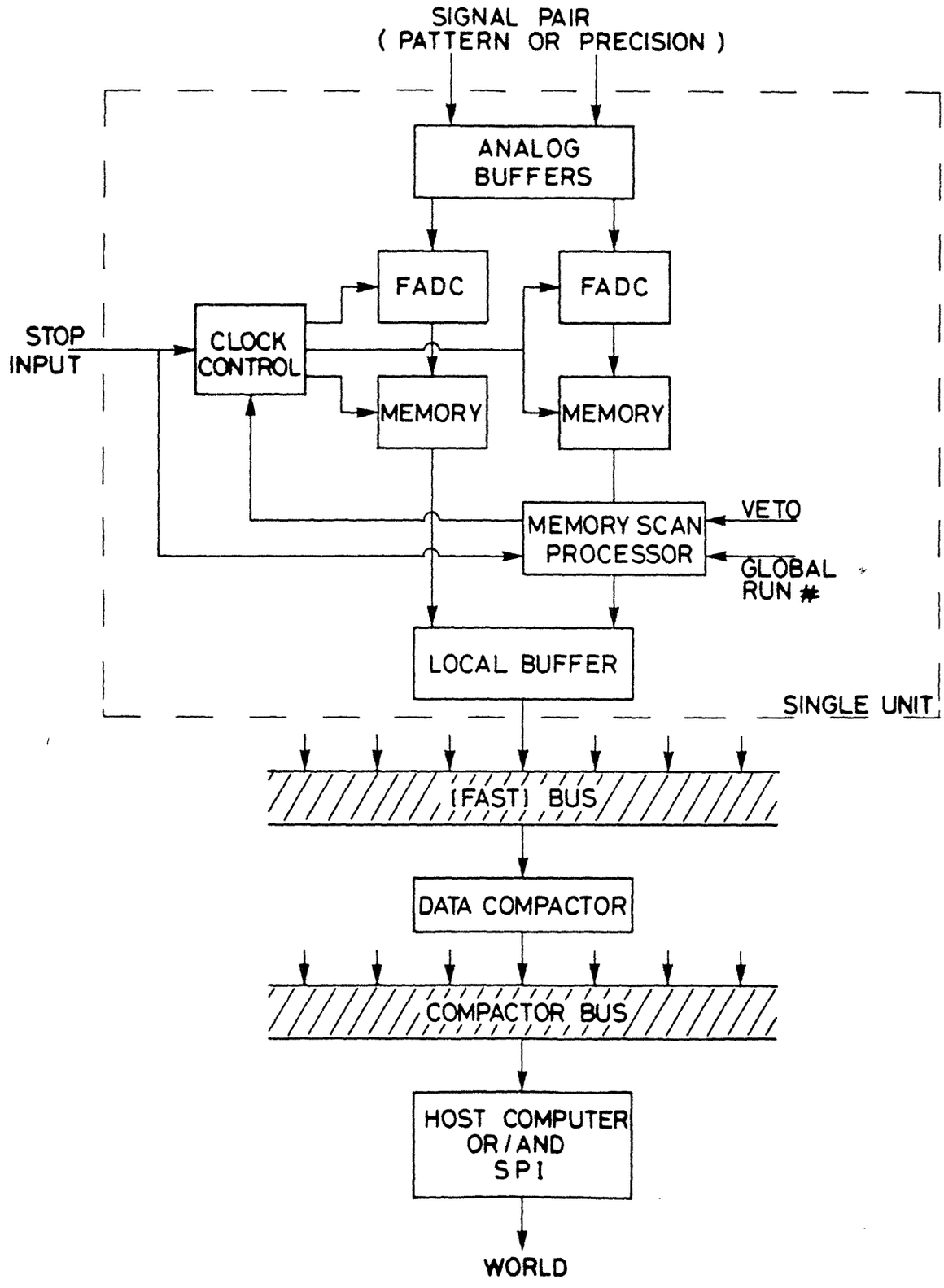


PATTERN WIRE (Fig. 1-B)

(Charge-Division Readout)



DATA FLOW


SIGNAL PAIR
(PATTERN OR PRECISION)
ANALOG BUFFERS
FADC
FADC
STOP INPUT
CLOCK CONTROL
MEMORY
MEMORY
VETO
MEMORY SCAN PROCESSOR
GLOBAL RUN #
LOCAL BUFFER
SINGLE UNIT
(FAST) BUS
DATA COMPACTOR
COMPACTOR BUS
HOST COMPUTER OR/AND SPI
WORLD