MASSACHUSETTS INSTITUTE OF TECHNOLOGY

LABORATORY FOR NUCLEAR SCIENCE REPORT

Technical Report Number 121 August 18, 1981

Dynamic Compensation of Small Errors in Drift Chamber Positioning Using an Optical CCD-based System

U. Becker, J. A. Paradiso

Laboratory for Nuclear Science, Massachusetts Institute of Technology,

Cambridge, Massachusetts, USA.

Abstract

We describe a fully digital and modular system for on-line monitoring and active compensation of small variations in position. We have applied this system to keep a 5 x 1.8 meter drift chamber frame planar. A linear 256-cell CCD array is used to obtain a positioning accuracy within one cell-width (13 μm). This system will enable a momentum measurement of $\leq$ 1% accuracy when the chamber is used in a magnetic field.

I) Introduction

Tracking high energy particles from the upcoming generation of colliders[1] through magnetic fields of 10-20 kgauss will pose new problems because of the extremely small deflections involved. Accuracy of survey measurements is essential for providing high resolution in detectors using precision drift chambers. For example, in a detector[2] for operation at future storage rings, 96 large drift-chamber packages (5 x 1.8 meters in area) will be mounted in equi-angular segments about the intersection region. This size, together with a 1% momentum resolution requirement at 50 GeV, is a considerable step up from present day central detectors[3]. To fully utilize the resolving power of drift chambers ($\sigma_D \simeq 150$ μm), the supporting structure must be reproducible to an amount $\Delta x << \sigma_D$. We also note that 50 GeV ray deflected by a 15 kG magnetic field will only produce a sagitta of 3000 μm, thus 1% measurements will require a determination of positioning within 30 μm. Stresses introduced via temperature variation, pressurization, gravitational and tensor forces, settling, etc., are expected to deform the chambers and affect the accuracy of the initial survey measurements over a long time period. To effectively confront this problem, we have developed a position-monitoring system employing optically sensitive charged-coupling-device (CCD) arrays. Even though a "digital" position monitoring device composed of discrete sensing cells is more elaborate than continuous analog designs[4], we chose the digital approach for long-term stability; i.e., the digital reading will be insensitive to long-term fluctuations due to temperature and other factors.

Figure 1 shows a sample drift chamber mounted in the detector[2]. Linear CCD arrays 256 cells long (13 μm/cell) are mounted opposite each corner of the chamber on stable, stress-free carrier rings. Light-emitting diodes affixed to the chamber are focused onto the corresponding CCD arrays. After installation and

initial surveying, the centroid of the focused LED illumination on all CCDs is recorded and stored via computer. The CCDs are periodically checked thereafter. A deflection of the chamber will change the position of the LED relative to the CCD and thus move the focused centroid. When a discrepancy is noticed, the computer brings the centroid back to its original value by restoring the chamber position with small motor drives under feedback control (labeled "adjust" in Figure 1). In this way, the deformation of individual chambers is compensated, and the planarity of the wire plane remains accurate.

Similar techniques of active compensation using a CCD position sensor have been sucessfully developed and applied in stellar tracking[5] and navigation[6] applications.

II) Electronics and Readout

Figure 2 shows a block diagram of the CCD readout system which was developed at MIT. There are 3 major system components; the controller, the distributor, and the driver/digitizer. The controller generates the complex clocking signals required to read the CCDs. It addresses one out of sixteen CCDs in each distributor, and stores a 2 x 256-bit digital rendition of the optical pattern detected by the selected CCD into self-contained buffer memory which may later be sequentially read via CAMAC.

The distributors generate necessary power supply voltages and fan out clocking signals to groups of 16 CCDs. When a distributor is "on-line", data and feedback signals from the addressed CCD only are routed to the controller along the bus. "Off-line", no clocking signals are fed to the CCDs and no signals are output over the bus. The distributors may be switched on- or off-line by CAMAC commands thus (putting only one distributor on-line at a time), the four addressing bits output from the controller specify a unique CCD.

The driver/digitizers are simple circuits required by each CCD which buffer

the clocking signals and digitize the video output of the CCD into 2 bits. We are presently using analog comparators as digitizers, creating 3 possible digital states (i.e., 0, 1, 3). The driver/digitizers also buffer an output which activates a light-emitting diode during a read sequence, creating light focused onto the corresponding CCD.

The controller is "daisy-chained" to the distributors by a 14-line bus, hence the system is easily expandable; the quantity of CCDs is fixed only by the number of distributors, which may be added arbitrarily to the system. We are presently clocking our CCDs in the range 20 → 50 KHz. This rate yields an integration period of 5 → 10 msec, which provides sufficient optical sensitivity for our applications, while still keeping the thermal "dark signal" manageable at room temperature. Using a simple Fortran program, a CCD is completely read into computer memory within 1/2 second; faster software can shorten this delay considerably.

The motor drives are computer-directed through CAMAC by a custom-built 16-channel motor controller. Each motor is uniquely addressable and can be set into motion (forward or reverse) and halted by CAMAC commands.

Further details on the hardware can be found in the Appendix.

III) Testing

Figure 3 shows photographs of the test setup. Photograph a) is an edge view of a prototype chamber frame, 1.5 x 5 meters in area. CCD/LED assemblies (as depicted in photo b)) are placed at the 4 corners of the frame and midway along either side. A motor drive (see photo c)) opens the jaws of a slotted piece of aluminum by elastic deformation. The jaw is prestressed at 400 lbs and will vary ±80 lbs during adjustment. These assemblies move the frame vertically ≃ ± 150 μm without backlash, and one is placed at each CCD/LED site. The CCD controller, distributor, and a prototype driver/digitizer are shown in photo d). The

entire configuration is manipulated through CAMAC by a PDP-11/03 microprocessor system.

Figure 4 shows the actual CCD output; the signal from the focused led is evident, and generally spans 10 → 20 CCD cells with our present optics (better resolution is obtained by removing the glass window over the CCD).

We have developed a simple computer program to test the feasibility of automatic position restoration as described in Section I. First, the centroids of all LEDs at the rest position are stored in computer memory. Next the frame is deflected, either by applying mechanical stress on the frame itself or by randomly torquing a motor drive. This shifts the position of the LED w.r.t. the CCD typically 50 → 100 μm, as monitored by precision deflection gauges affixed to the test frame. By incrementally moving the motor associated with the deflected portion of the frame, the centroid of LED illumination can be restored to its previous value. This process has repeatedly brought the frame back to within an average of ±5 μm (±10 μm on extreme) of the original, undeflected position (as measured by the gauges) compatible with the granularity expected from the 13 μm CCD cell width.

Figure 5 shows the response of the compensation system to deflection caused by a 10 kg load*. The load was introduced at T = 3 seconds (as indicated), and deflected the frame ≈ 85 μm. The compensation program immediately began stepping the motor drive; however, after two pre-programmed search steps the computer realized it was moving the frame in the wrong direction and reversed the

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*) The internal stresses of the frame are small compared to this. For example, loading one unsupported corner with 10 kg gave a deflection of 0.7 cm, showing that the restoring moments are small compared to the 10 kg loads used in these tests.

motion at T = 10 seconds. After each crossing of the reference position, the motor step size was decreased and the direction reversed until a final convergence was reached at T = 50 seconds, where the frame was restored to within 5 μm of the reference. At T = 59 seconds, the 10 kg weight was removed (as indicated), now causing the frame to deflect ≃ 90 μm in the opposite direction. The compensation program was invoked, and at T = 90 seconds the frame was again restored to within 5 μm of the reference position. The compensation program was purposefully slowed in this test in order to enable manual reading of the deflection gauges; convergence to the reference position is normally achieved within 20 → 30 secs.

A schematic of the test frame configuration is given in Fig. 6, showing the location of the 6 CCD/LED sites and motor drives. In the test of Fig. 7, the frame was continually scanned, and resulting averaged positions at 1-minute intervals are plotted for all sites in units of CCD cells. Whenever a deviation of > 0.7 CCD cell from the reference (dotted lines) was detected, the compensation routine was automatically invoked, and the frame was restored. At T = 4 minutes, a 10 kg weight was applied at site #1; this is seen to have deflected both site #1 and the adjacent site #6 (the corner of the frame near site #6 was particularly elastic). At T = 5 minutes, these deflections are already compensated, and both sites are back at the reference positions. The 10 kg loads were successively applied to the remaining corners (sites #6, 3, and 4; see Fig. 6), as indicated; the resulting deflections were all compensated, and at T > 16 minutes the frame is seen to be stable at the reference positions, although 10 kg loads are present at all 4 corners.

Figure 8a) shows the mean positions of the focused centroids (read by the CCDs) for all 6 sites, plotted in units of CCD cells as a function of time over a 24-hour period. The CCDs were sampled every 15 seconds, and the averaged positions (as plotted) were calculated every 15 minutes. Gradual shifts in the mean positions can be noticed, due to temperature variations, etc. Figure 8b) is analogous to

Figure 8a); however, during this 24-hour period the computer program was instructed to restore each centroid to its original position (via the motor drives) whenever a deviation in the 15-minute averages of > 0.5 CCD cell was detected, thus compensating for the gradual motion of the frame and keeping it centered at the reference positions.

IV Conclusions

We have developed a digital position monitoring system with long-term stability and active feedback, which is insensitive to environmental influences and can keep a drift chamber plane in place within ±10 μm. This feature is necessary for precision momentum determination of highly energetic tracks. After an initial calibration (by laser[7], for example) long-term stability is required for computer reconstruction. However, since huge mechanical structures, even if tempered, will always "work" internally, active compensation will be necessary. We point out that these considerations apply to all large precision chambers, and not only to the specific geometry mentioned.

APPENDIX: HARDWARE DETAILS

A) The Controller

A block diagram of the controller is shown in Figure 9. There are three somewhat independent sections of this circuit:

The CCD Distributor Addressing Latch

This is a 4-bit latch (7475-L4) which loads the 4-bit CAMAC "A" field when an F9, C, or Z is sent to the controller. The output of this latch is buffered via emitter-followers and is sent over lines Bus #1 → Bus #4 (and displayed via LEDs).

The CCD Clocking Circuitry

Two oscillators are used as clocking sources; oscillator CLK1 is preset via an on-board trimmer potentiometer, while CLK2 can be adjusted via an external potentiometer on the front panel. The CLK Source selector switch (S3) enables one to select either clock. One may also set the switch in a "null" position, thus enabling an external clocking pulse to be input via the "ext clk" connector.

The clock source is introduced into the CCD clocking circuitry. This is a complex arrangement of gates, flip-flops, and counters which is described in the Fairchild CCD-110 application notes[8]; I won't discuss the details here. The 5 output signals are buffered via transistors and output onto lines Bus #5 → Bus #9.

The CCD Control and Readout Circuitry:

This comprises the major portion of the apparatus. Three

CAMAC commands are accepted: an F0, an F2, and and F9. They are decoded by a 74154 demultiplexor.

Upon receipt of an F0, the read sequence starts. All processes are timed via the $V_{\phi XB}$ and $V_{\phi R}$ signals fed back from the CCD driver/digitizer to guarantee synchronism. The read sequence is itemized below and depicted in a timing diagram (Figure 10).

i) CAMAC N • F0 • S1 sent

ii) Readout latch (L1, 74279) is set. This holds the output latch open (L3, 7475), and enables the fed-back $V_{\phi XB}$ pulses to clock counter C1 (7493). [The $V_{\phi XB}$ pulses are output at the beginning of each cycle through the CCD.] The V_{LED} bus line (Bus #10) goes high; this triggers the LEDs, illuminating the CCDs attached to any distributors that are currently on-line.

iii) Nothing else happens for the first 4 cycles through the CCD; only counter C1 is advanced. This is done to avoid any transient effects. At the start of the fifth cycle (≥ 4 $V_{\phi XB}$ pulses), the $V_{\phi R}$ pulses are allowed to clock counter C2 (the $V_{\phi R}$ pulses go high for each "cell" of video data output). These $V_{\phi R}$ pulses first trigger a monostable trigger delay (P1-555) which shifts the phase and broadens pulse-width such that the video data is sampled in the center of each "cell" (see below).

iv) Nothing happens for the first 3 $V_{\phi R}$ pulses; only counter C2 is advanced. This delay is introduced since the first 3 video cells are supposedly "dummies", i.e., they contain no video data, and are required to advance the data through the analog shift register inside the CCD. After the 3rd $V_{\phi R}$ pulse, the delayed $V_{\phi R}$ pulses are allowed to advance counter C3 and are input to a pulse

generator (P2), creating the shift register gate. This is a narrow (≃ 500 nsec) pulse which clocks the shift register in the middle of each "cell" of video data (the 2 data bits--DATA 0, DATA 1--from Bus #3 and Bus #4 are input to the shift register).

v) The shift register and counter C3 are clocked for the next 256 $V_{\emptyset R}$ pulses. After the 256th pulse, the $V_{\emptyset R}$ pulses are inhibited from further advancing either counter C3 or the shift register.

vi) Nothing happens until the 5th $V_{\emptyset XB}$ pulse is received. At this time the "data present" latch (L2) is set and a "reset" pulse is created which clears all counters (C1 → C3) and resets the readout latch. This closes the output latch (L3) and inhibits all further clocking pulses (V_{LED} is also brought low). The readout sequence is now complete, and the module may be sequentially read into computer via CAMAC.

Data from the shift register is read cell by cell into CAMAC via the F2 function--"read and advance." The CAMAC F2 is gated by the readout latch (V_{LED}) output and the reset timer (P3). If either a readout is in progress or the module is resetting itself (these define a "busy" criterion), the CAMAC F2 will have no effect, and the module will return X = 0 and Q = 0.

If the controller is not busy, a CAMAC F2 will first open the output latch, allowing the current data to be written onto CAMAC read lines R1 (DATA 0) and R2 (DATA 1). Upon receipt of F2 • S2 (later in the CAMAC cycle), the shift register is cycled and counter C3 is advanced. If counter C3 is advanced to 256, all further shift-register advance pulses are inhibited. The data present latch governs the "Q"

response of the F2 command. After an F0 readout sequence has been completed, this latch is set. Upon receipt of an F2 (provided the controller is not busy) it will respond with Q = 1 and X = 1. If 256 reads have been attempted, the next read (i.e., shift-register advance) will clear the data present latch, but will still answer Q = 1, X = 1; however all subsequent F2s will yield Q = 0, X = 1. Thus, one can read this module in a "halt on Q" mode, but in this case 257 words will be read, the last word being a "dummy" required to reset the data present latch.

The manual shift-register advance pushbutton emulates a CAMAC F2 and allows one to advance and examine the memory manually.

After the controller's memory has been read and emptied, a CAMAC clear is required before sending another F0 and starting the sequence anew. This can be done by a CAMAC C, Z, or F9--all are or'ed together (there is no manual "clear" on the controller). This resets all counters and latches (and loads the CAMAC "A" field into the distributor address latch; of course, for C and Z this field is zero) and returns the controller to a "ready" state.

B) The Distributor

The distributor performs essentially 3 tasks:

- buffers and fans out all CCD clocking voltages (including V_{LED}) to 16 ports
- effectively multiplexes the return signals from the 16 ports (i.e., each port is uniquely addressable)
- supplies the voltages required by the driver/digitizer modules.

The design of this circuit is extremely simple, but it is complicated by the 16-fold redundancy. Figure 11 shows the block diagram.

The on/off-line state of the unit is defined via an RS latch. The latch is set (on-line) by the CAMAC F1 bit or the on-line position of switch S1. The latch is reset (off-line) by the CAMAC F2 bit, a CAMAC C or Z, or the off-line position of switch S1 (note that the F1 and F2 bits only are used to simplify command decoding--hence, an F3, an F7, etc., will have undefined effects).

The CCD clocking signals and V_{LED} (Bus #5 → Bus #10) are first Schmidt-trigger conditioned and gated by the output of the latch; thereupon they are routed through a driver to 16 separate buffers and appear at B5 → B10 of each port. Because these signals are gated by the latch, no signals appear at the 16 ports when the module is off-line. When the module is on-line, however, these signals will be present at all 16 ports.

There are 4 signals (B1 → B4; 2 data + 2 feedback) received from the addressed port which are written onto lines Bus #1 → Bus #4. These 4 signals are first Schmidt-trigger conditioned at all 16 ports and then brought to the inputs of four 16-to-1 data selectors (74150) which have common addressing lines derived from Bus #11 → Bus #14 (from the distributor address latch in the controller). The output of each of these selectors is brought to the bus via an open-collector driver. The data selectors are all gated by the latch output; when the unit is off-line, the data selectors will not pass data and are effectively "disconnected" from the bus write lines. When the unit is on-line, the data selectors pass data from the addressed port, and it is written onto the bus.

The CCD power supply is very straightforward. The -6 volts comes straight from CAMAC with no buffering or decoding (one must be careful; the -6-volt line in any CAMAC crate containing CCD

distributors might be a bit noisy). The +15 and +8 volt supplies are derived from the CAMAC +24 volts via integrated circuit regulators (the 7815 and 7808 are used respectively). These power supply voltages always appear at the 16 ports regardless of the on/off-line state of the distributor.

There are 2 bus connectors at the rear of the module (i.e., IN-OUT). Both are in parallel--it doesn't matter which is used for input and which is used for output.

C) The Driver/Digitizer

This unit plugs into an output port of a distributor (via ribbon cable) and performs 3 general functions:

- buffers the 5 CCD clocking signals and shifts their swing to 0 → 7 volts before applying them to the CCD (also feeds back $V_{\phi XB}$ and $V_{\phi R}$).
- digitizes the video output of the CCD (via comparators) into 2 bits.
- buffers V_{LED} (B1) and provides a variable LED driver; an LED can be attached which flashes on when a readout is in progress, and can be focused onto the CCD.

This circuit is exceedingly simple--purposely so, since one is required with each CCD. There are only 6 chips present, counting the CCD. Four transistors are also used; however, there are 3 indicator diodes included in the package which should be eliminated when the circuit is built on a production basis. This will reduce current draw and eliminate 2 of the transistors (which are used as LED drivers).

The block diagram is portrayed in Figure 12. The 6 signals

received from the cable (B5 → B10) are first conditioned and inverted by Schmidt triggers and then routed through open-collector drivers where they are shifted to 0 → 7 volts and fed to the CCD (with the exception of B10, V_{LED}). The $V_{\emptyset XB}$ and $V_{\emptyset R}$ signals are fed back onto B1 and B2 respectively. V_{LED} is fed through a series of buffers and drives the "active" LED indicator and an emitter-follower with base-voltage varied by trimmer T1. An LED can be plugged into the "LED output" connector which is fed via this emitter-follower; thus T1 varies its brightness, and it is illuminated only when a readout sequence is in progress.

The video output of the CCD is first isolated via an emitter-follower and then applied to two analog comparators. These are fast LM318 operational amplifiers, and the threshold of each is set independently via trimpots T2 and T3. The outputs of these comparators are monitored by 2 LEDs and clamped 0 → 5 volts through zener diodes before being fed to TTL buffers which invert these signals and feed them onto B3 (DATA 1) and B4 (DATA 0). Since comparators are used for digital conditioning, only 3 states are possible:

Both comparators below threshold (0, 0)

One comparator above threshold (0, 1)

Both comparators above threshold (1, 1).

The state (1, 0) does not exist independently.

This driver/digitizer circuit can easily be altered, and other approaches can be examined; i.e., simple A → D converters can replace the analog comparators (yielding a more precise digital rendition of the video waveform), the trimpots can be eliminated by a biasing newtwork, the CCD video signal can be preamplified before being applied to the

comparators (thus reducing threshold shift caused by drifting input of offset current in the OP-Amps), etc.

D) The Motor Controller/Driver

This circuit enables the computer to address 1-out-of-16 motor drives, and set it into "Forward," or "Reverse," motion. The block diagram is given in Figure 13. The Forward and Reverse commands (F7 and F8) gate the CAMAC A-field into latch L2 which drives a 4-to-16-line address decoder, thus enabling the 4-bit A-field to specify 1-out-of-16 outputs. The F7 and F8 commands also set latch L1 which gates the address decoder; when L1 is set, the address decoder is enabled and the output line specified by the CAMAC A-field is asserted. The F9, C, and Z commands reset L1, and thus inhibit all address decoder output lines. Switch S1 overrides the output of L1, thus providing a manual motor control. Switches S3 → S5 are Or'ed into the output of L2, and provide a manual motor address select. In addition, the F8 command is also input to latch L3. This latch is gated by all accepted CAMAC commands; however, it is set only when an F8 is sent, and thus is used as a "Forward/Reverse" control line (switch S2 provides a manual override). The address decoder outputs feed the "enable" inputs of "Analog Converters," and the output of L3 is fed to the "Forward/Reverse" inputs of these modules. The "Analog Converters" are simple circuits which enable digital control of a 3-state analog output, and have the transfer function:

Logic Inputs		Analog
Enable	F/R	Output Voltage
1	1	-15
1	0	+15
0	(anything)	0

The outputs of the analog converters are buffered by driver transistors, and power the motors. Simple DC motors are used, and move the frame +/- 150 μm by means of an elementary lever-wedge assembly.

In summary, an F7 • A_n sets motor #n into forward motion, an F8 • A_n sets motor #n into reverse motion, and an F9, C, or Z halts all motors. Only one motor may be controlled at a time with this circuit.

E) The General Software Approach

The details of software implementation are up to the "systems engineers," but here I'll sketch a general plan for CCD readout which might, in some form, be applied. A flow chart is given in Figure 14.

First one generates a CAMAC "Z" cycle on all crates to turn all of the distributors off-line. Then an F1 is sent to the selected distributor (containing the selected CCD) to turn it (and only it) on-line. Thereupon an F9 • A_n (where A_n is the address of the CCD relative to the distributor, in the range $0 \rightarrow 15$) is sent to the CCD controller to clear all internal counters and registers and to load the distributor address register with the desired CCD address. An iteration counter "ITMS" is zeroed, and we send the "initiate readout" F0 command to

the controller. Immediately afterwards, we begin sending F2 commands to the controller--if it responds X = 0, Q = 0, we know it is not yet ready and still busy with the readout, so F2 is tried again. If the controller remains busy after some enormous amount of readout attempts (say, 2000), we have detected a problem and declare a "time-out" situation. This generally occurs because the $V_{\emptyset R}$ and $V_{\emptyset XB}$ clocking pulses (Bus #1 and #2) are not being fed back properly. Check the following:

- Is the CLK-ON switch on the controller ON? If so, it should be on "AUTO"!!
- Is the distributor on-line and properly attached to the bus? Is the controller properly tied to the bus?
- Is the CLK SOURCE switch on the controller set to CLK1 or CLK2? If it is set to "ext", is a clocking pulse input via the "EXT CLK" connector?
- Is a CCD driver/digitizer plugged into the addressed port on the distributor?

If none of the above is true there exists a hardware problem, and some tracing might be required to track it down (bad cable?). If a "time-out" exists, the controller can still be cleared via an F9, and another CCD may be read out.

When the controller is "ready," the rest of the 256 words are read out via F2 (if "stop-on-Q" is used, 257 total words are read out--the last read is a "dummy"). The 256 words (actually only 2 bits/word here!) are then processed according to the particular application in mind. The scenario may now be repeated, and the next CCD may be specified and read out.

Acknowledgements

We are grateful to Profs. S.C.C. Ting, J.I. Friedman, and Dr. F.J. Eppling for valuable advice and support. We are happy to thank Ron Hoffmann, Peter Berges, Dave Osborne, Jim Donahue, and Paula Reddick for their technical assistance.

References

1) "A Proton-Proton Colliding Beam Facility," BNL 50718 (1978).
Design Report, FNAL Superconducting Accelerator (1979).
"Design Study of a 15 to 100 GeV e^+e^- Colliding Beam Machine (LEP)," CERN/ISR-LEP/78-17 (1978).

2) MIT Large Detector Study, presented to the BNL ISA workshop by S.C.C. Ting, U. Becker, and D. Luckey (July 1981).

3) A. Wagner, Central Detectors, DESY Preprint 80/83 (1980).

4) S.J. Bailey, Control Eng. 26, No. 12, 27 (1979).

5) R.H. Stanton and R.E. Hill, J. Guidance and Control 3, No. 2, 179 (1980).

6) P.M. Salomon, Optical Eng. 20, No. 1, 135 (1981).

7) H. Hilke, "Status and Prospects of Laser Beam Calibration," contribution to the wire chamber group of the BNL ISA workshop (July 1981).

8) Application notes for Fairchild CCD 110 and CCD 111, Fairchild, Inc.

FIGURE CAPTIONS

Fig. 1 Cross-sectional view of a drift chamber mounted in the detector[2]. The LED/CCD configurations are shown, and the motor drives are labeled "adjust".

Fig. 2 Block diagram of the CCD readout configuration.

Fig. 3 a) Photograph of the test frame (1.5 x 5 meters in area).

b) A CCD/LED assembly; light from the LED (mounted on the frame) is focused onto the CCD (mounted on a bracket fixed to the floor) via a cylindrical lens.

c) A computer-controlled motor drive, capable of moving the frame vertically $\simeq \pm 150$ μm.

d) CCD readout electronics. The CCD controller and a distributor are mounted in the CAMAC crate, and a prototype driver/digitizer is seen in the foreground.

Fig. 4 CCD video signal (lower trace) and a digitized comparator output (upper trace) arising from focused LED illumination (see insert). Photo a) shows an entire cycle through the CCD (256 cells), while photo b) has an expanded time scale and shows outputs from individual CCD cells.

Fig. 5 Response of the compensation system to the "step" impulse created by a 10 kg load. Fig. 5a) shows the frame position as read by the CCD and computer (in units of CCD cells) while Fig. 5b) shows the frame position as read by the mechanical deflection gauge (in μm) at the CCD/LED site. The compensation system is seen to restore the frame to within 5 μm of the reference position (horizontal dotted line) in both cases.

FIGURE CAPTIONS

(continued)

Fig. 6 Sketch of test frame configuration, showing CCD/LED/motor sites. The vertical lines represent drift wires (the actual drift wire density is 11 cm). CCD/LED/motor sites are located at the 4 corners of the frame and midway along either side (where the drift wire supports are mounted), thus monitor the position of the drift wire plane.

Fig. 7 Response of all 6 CCD/LED sites to 10 kg loads successively placed at each corner of the frame. The CCD's were scanned continuously, and mean positions were calculated and plotted each minute. The site #'s at which loads were placed are indicated at the bottom of the figure. The positions are plotted in units of CCD cells (as read by the computer). The response of site #4 to the 10 kg load is opposite to that of the other sites; this is because the CCD at site #4 is inverted with respect to the scale convention.

Fig. 8 Average centroid positions (integrated over 15-minute intervals, sampling each CCD every 15 seconds) as a function of time over a 24-hour period. In Fig. 8a), the internal motion of the frame was uncompensated; in Fig. 8b), the motor drives were used to restore the centroids to the reference positions whenever deviations of > 0.5 CCD cell were detected. The vertical axes are in units of CCD cell-width (at 13 μm/CCD cell).

Fig. 9 Block diagram of the CCD controller electronics.

FIGURE CAPTIONS

(continued)

Fig. 10 Timing diagram for the CCD readout sequence, initiated by a CAMAC F0.

Fig. 11 Block diagram of the CCD distributor electronics.

Fig. 12 Block diagram of the CCD driver/digitizer electronics.

Fig. 13 Block diagram of the motor controller/driver electronics.

Fig. 14 Sample flow chart of a possible software handler for CCD readout.

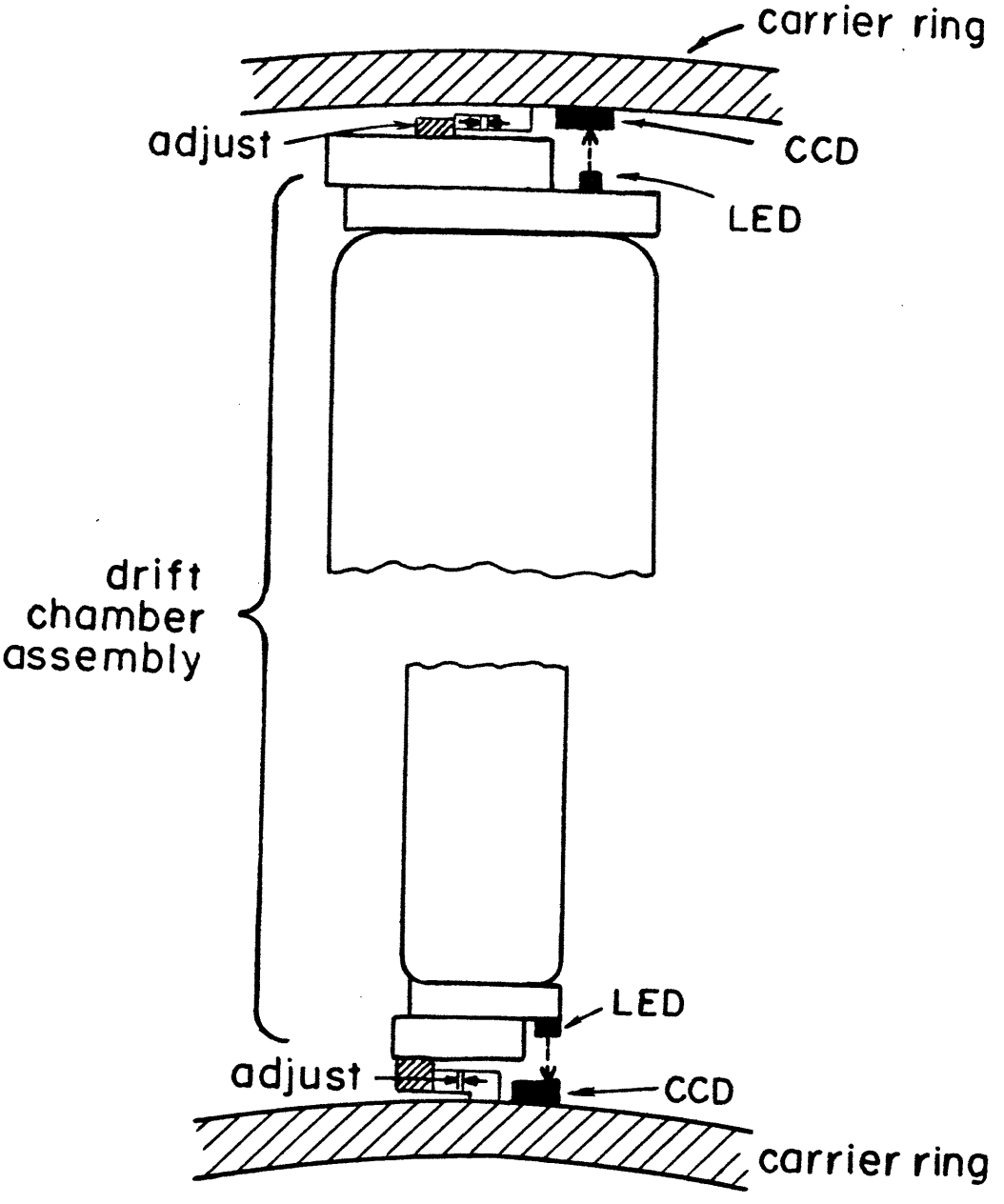

carrier ring
adjust
CCD
LED
drift
chamber
assembly
LED
adjust
CCD
carrier ring

FIGURE 1

CCD SYSTEM - GENERAL CONFIGURATION

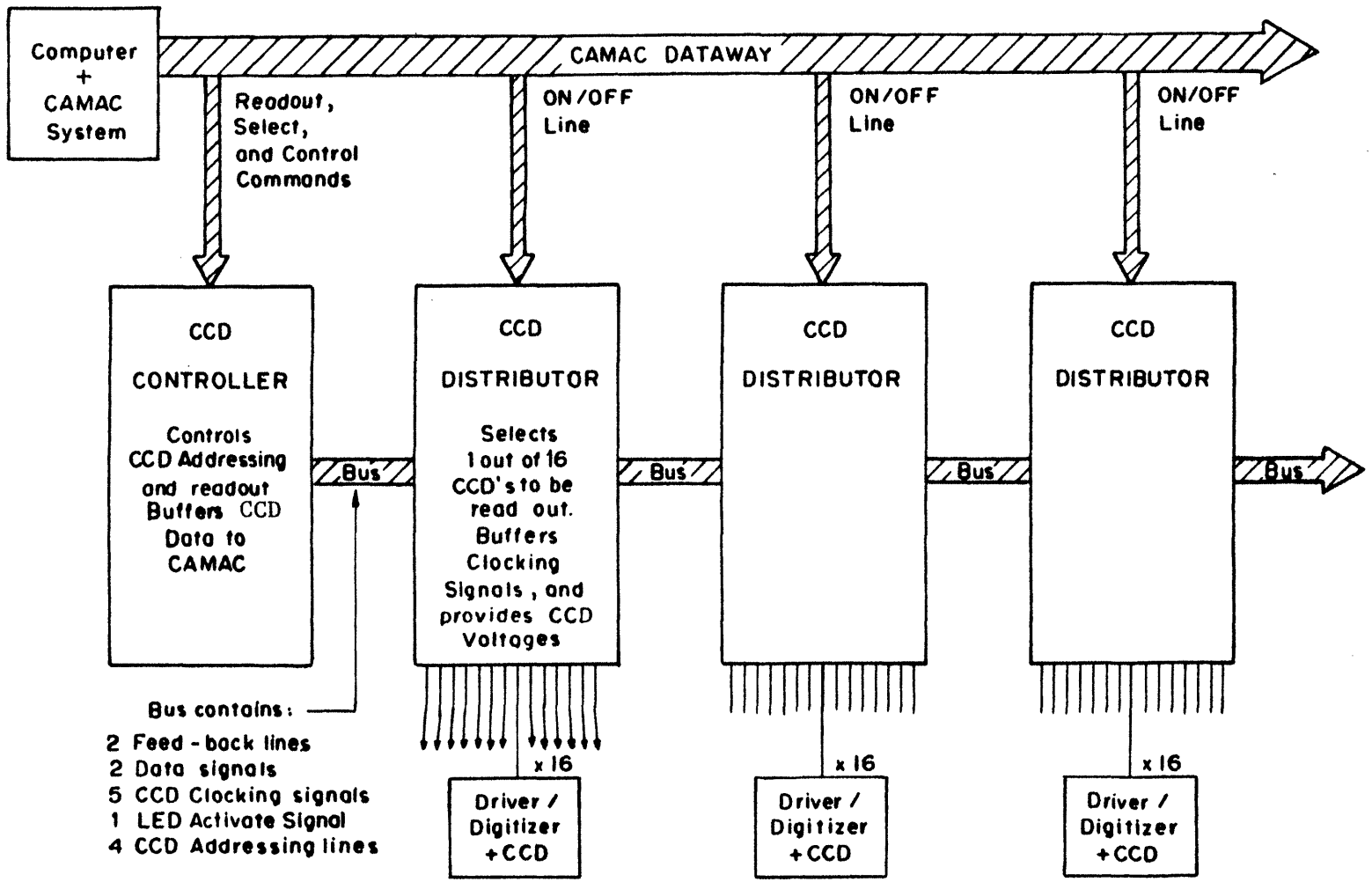
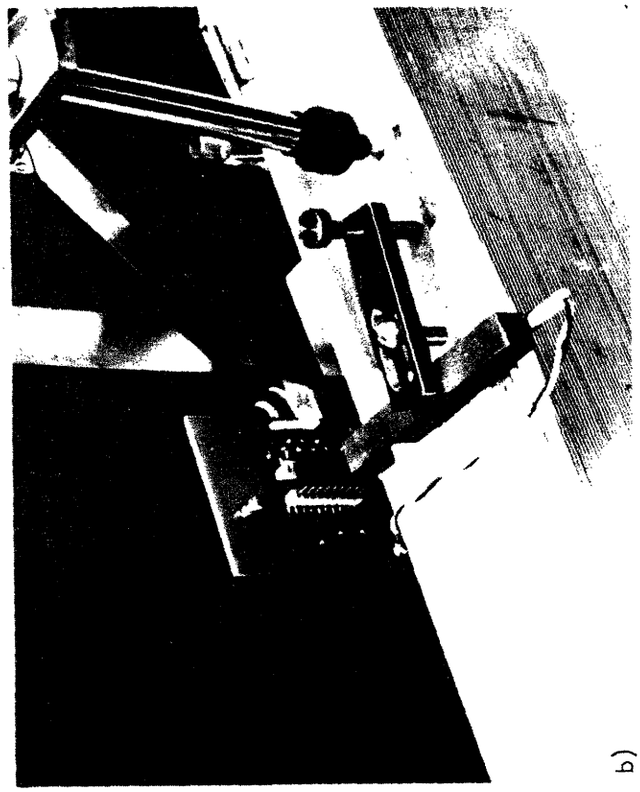
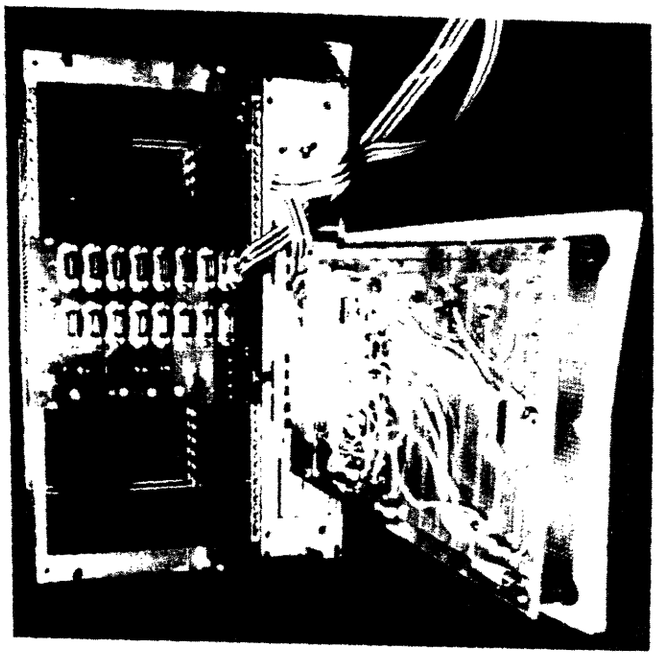


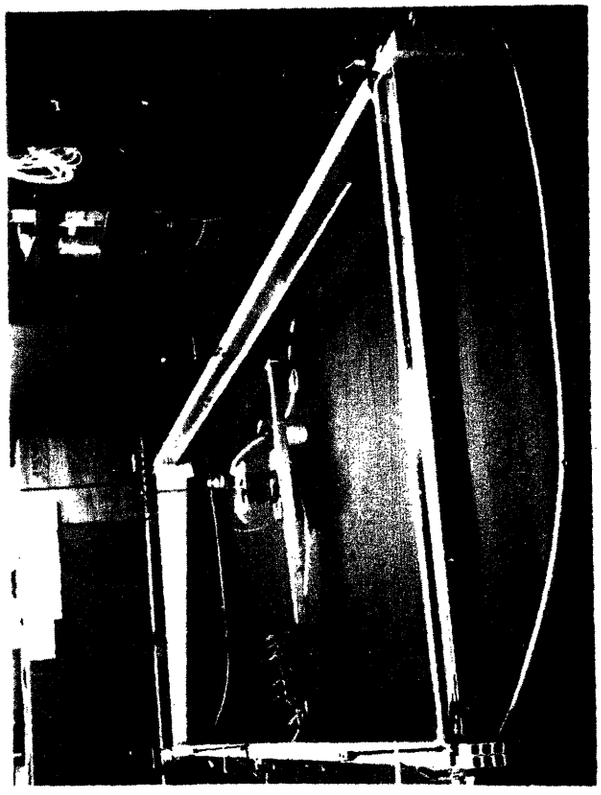
FIGURE 2



b)



d)



a)

c)

FIGURE 3

CCD RESPONSE TO FOCUSED LED ILLUMINATION

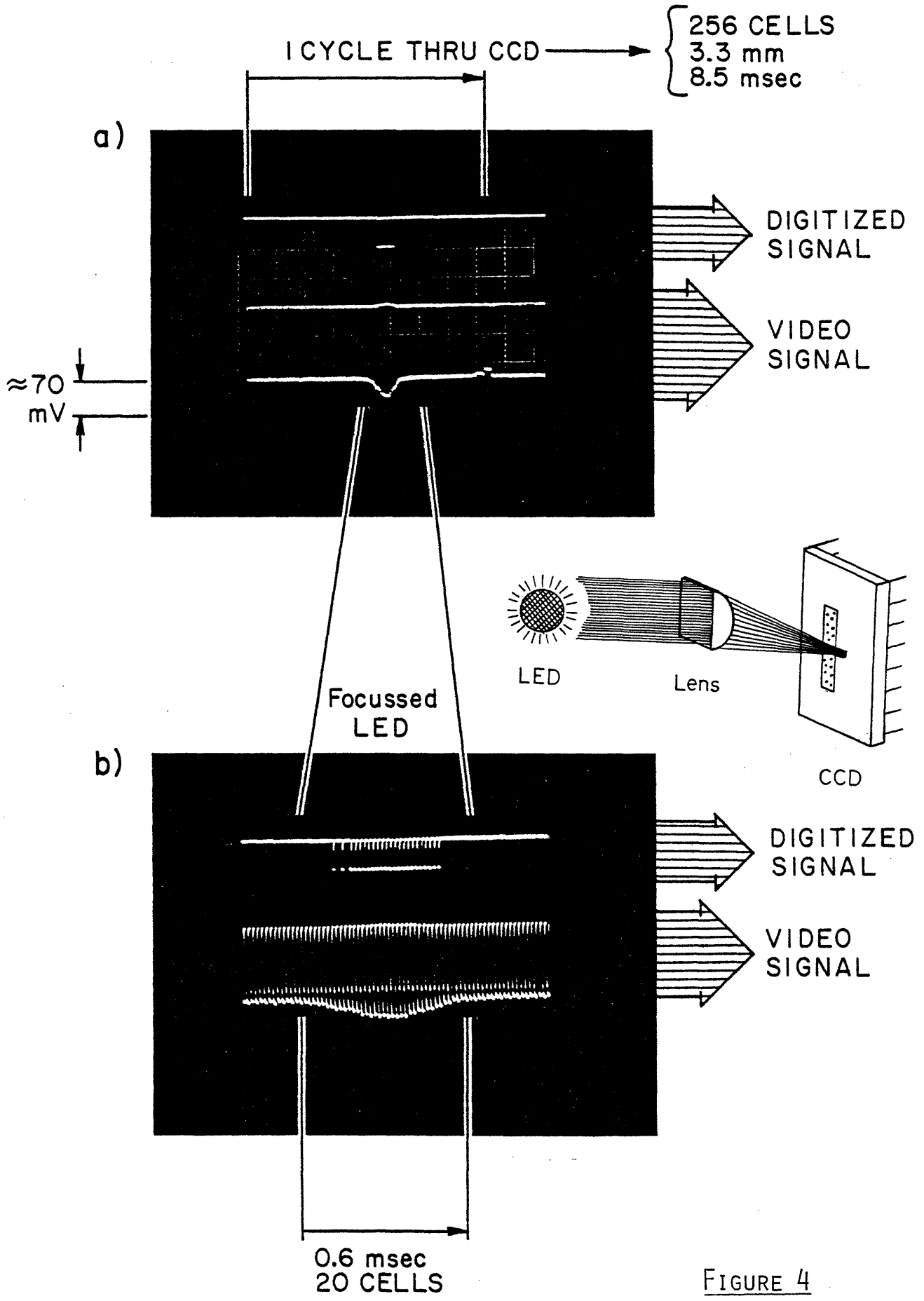


FIGURE 4

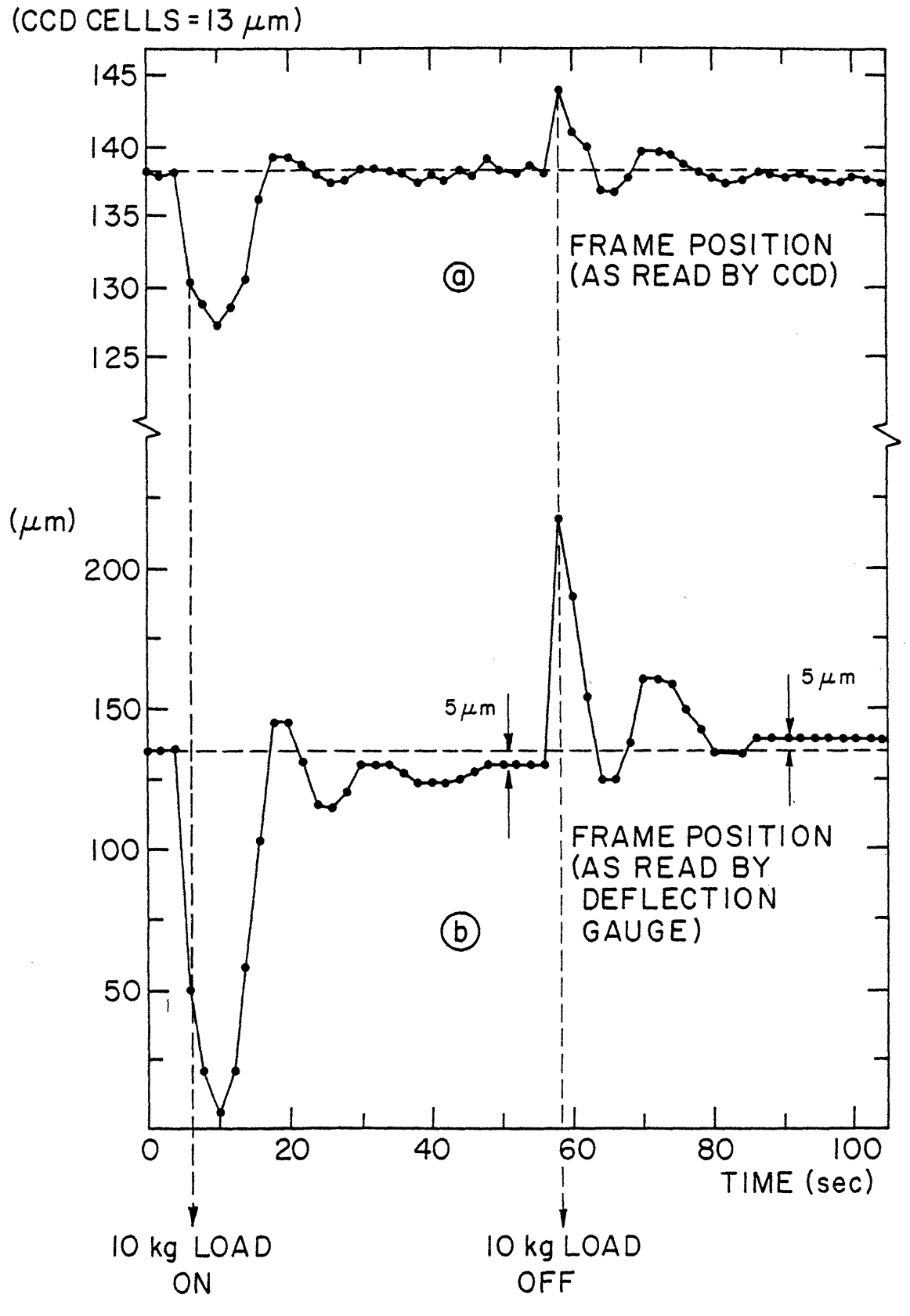
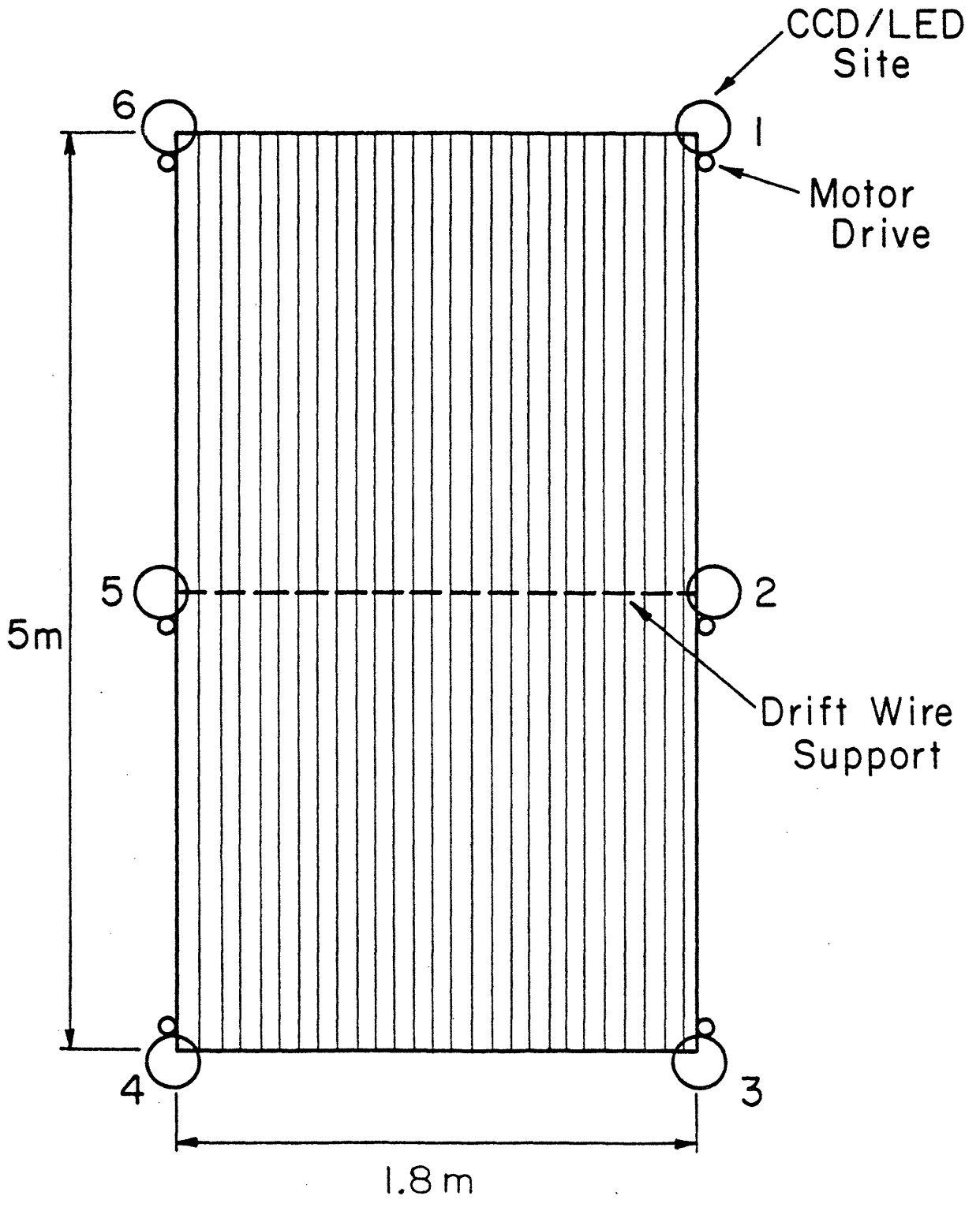

STEP RESPONSE
(CCD CELLS = 13 μm)
145
140
135
130
125
(μm)
200
150
100
50
FRAME POSITION
(AS READ BY CCD)
ⓐ
5 μm
5 μm
FRAME POSITION
(AS READ BY
DEFLECTION
GAUGE)
ⓑ
0
20
40
60
80
100
TIME (sec)
10 kg LOAD
ON
10 kg LOAD
OFF

FIGURE 5

FIGURE 6



TEST FRAME (TOP VIEW)

LOAD/COMPENSATION TEST

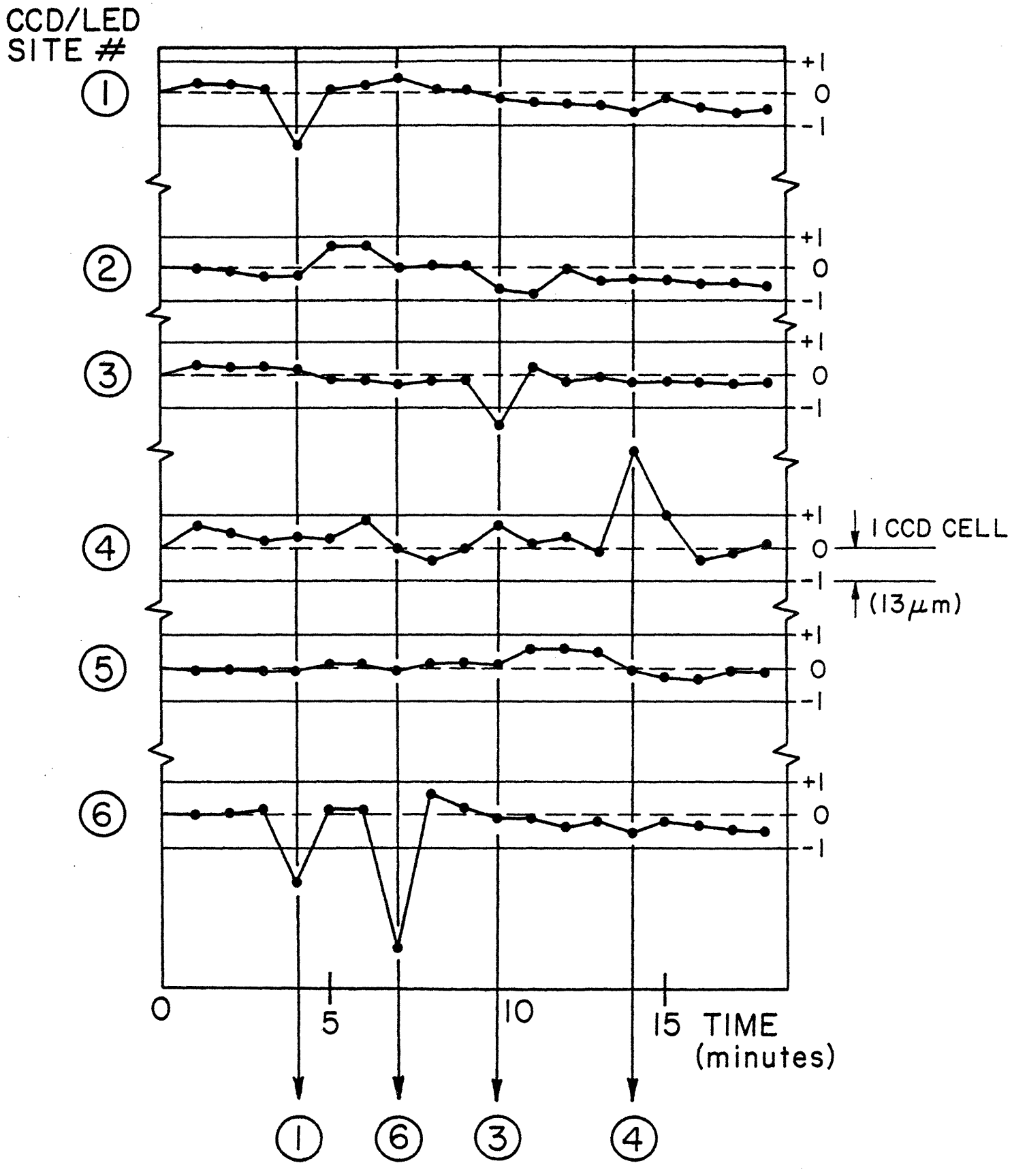
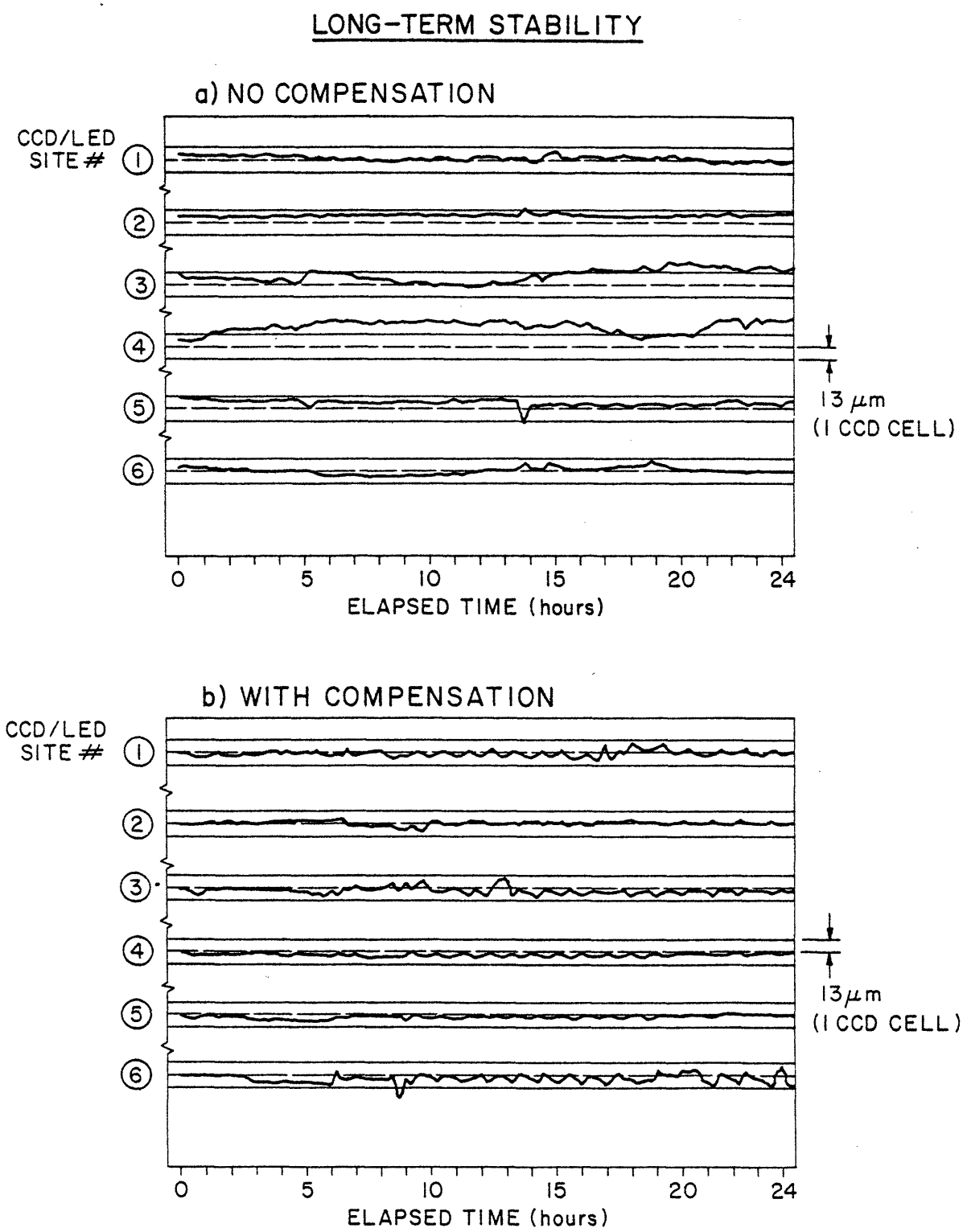


FIGURE 7

FIGURE 8


LONG-TERM STABILITY
a) NO COMPENSATION
CCD/LED SITE #
1
2
3
4
5
6
13 μm
(1 CCD CELL)
0
5
10
15
20
24
ELAPSED TIME (hours)
b) WITH COMPENSATION
CCD/LED SITE #
1
2
3
4
5
6
13μm
(1 CCD CELL)
0
5
10
15
20
24
ELAPSED TIME (hours)

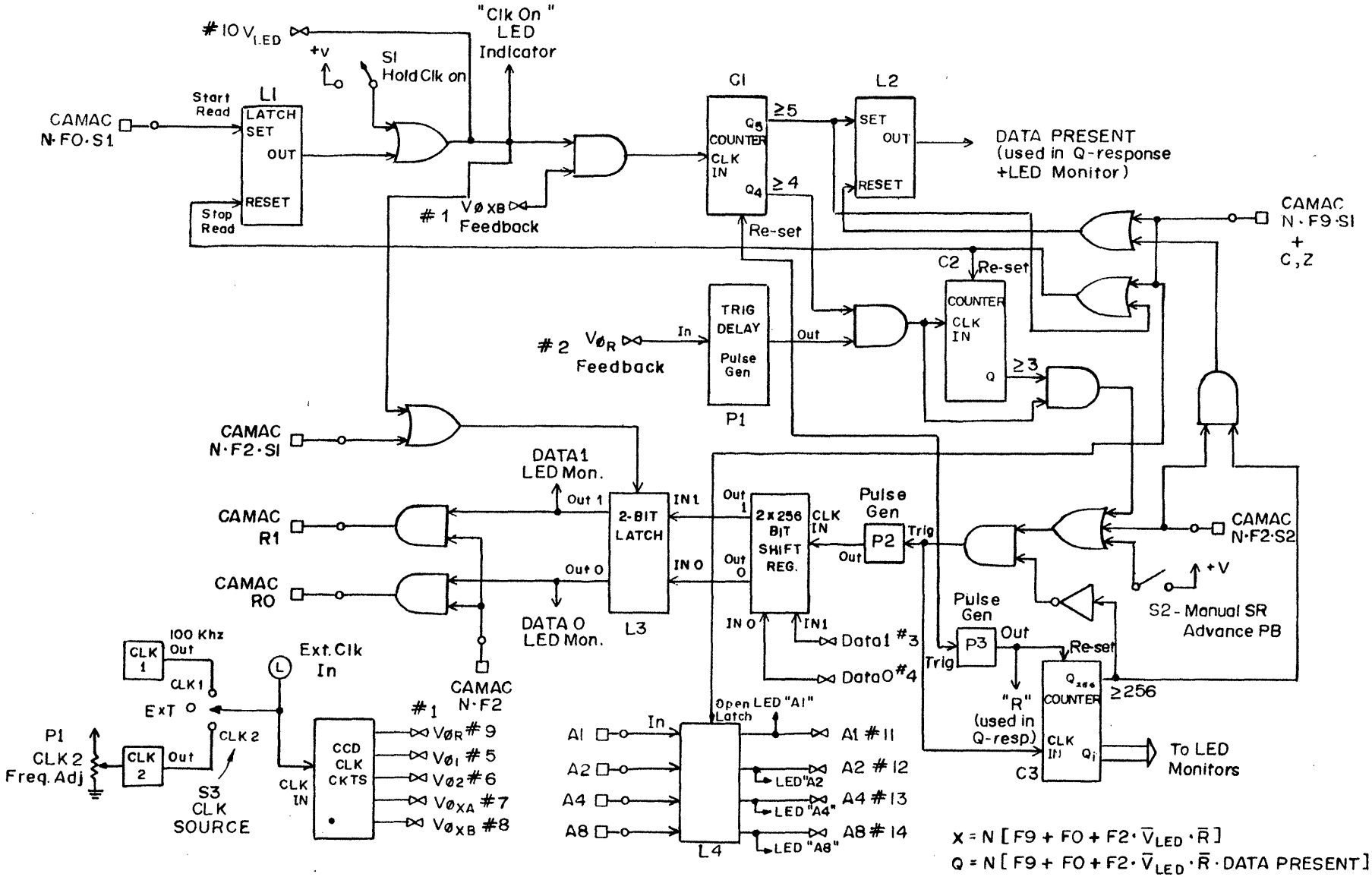


FIGURE 9

CCD CONTROLLER
BLOCK DIAGRAM

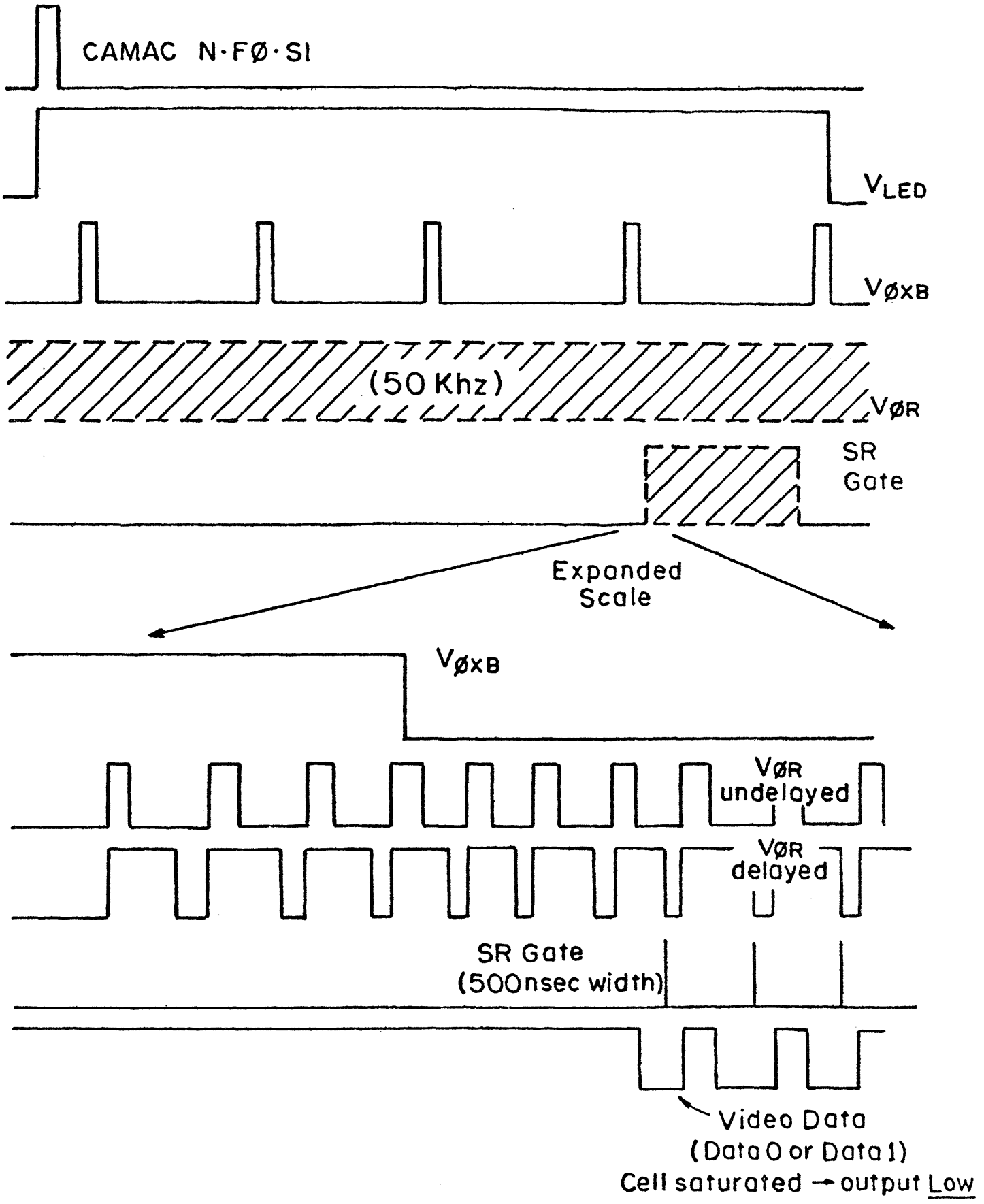
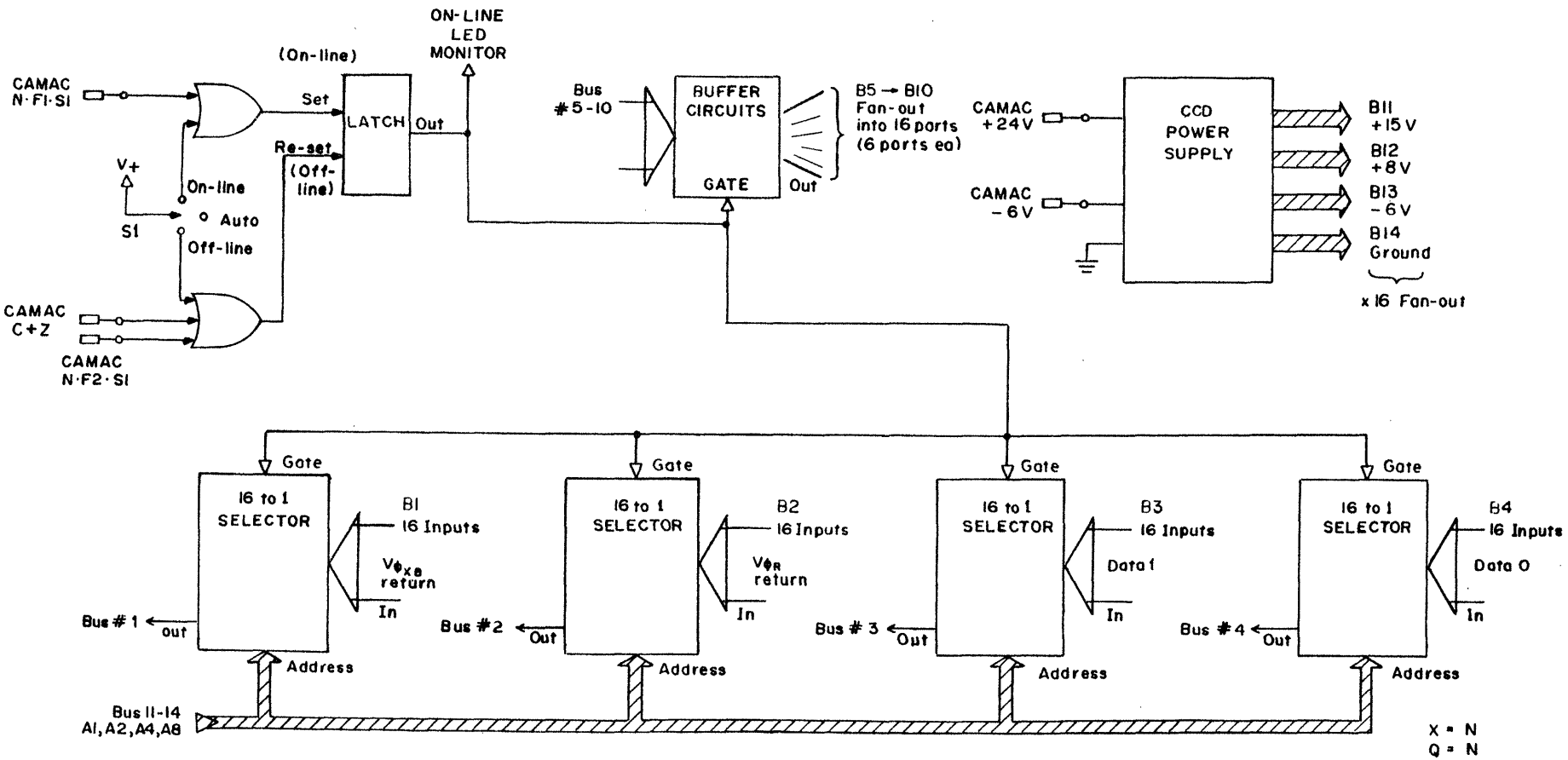

READOUT SEQUENCE – TIMING DIAGRAM
CAMAC N·FØ·SI
VLED
VØXB
(50 Khz)
VØR
SR
Gate
Expanded
Scale
VØXB
VØR
undelayed
VØR
delayed
SR Gate
(500nsec width)
Video Data
(Data 0 or Data 1)
Cell saturated → output Low

FIGURE 10

FIGURE 11

CCD DISTRIBUTOR-BLOCK DIAGRAM



CCD DRIVER/DIGITIZER

BLOCK DIAGRAM

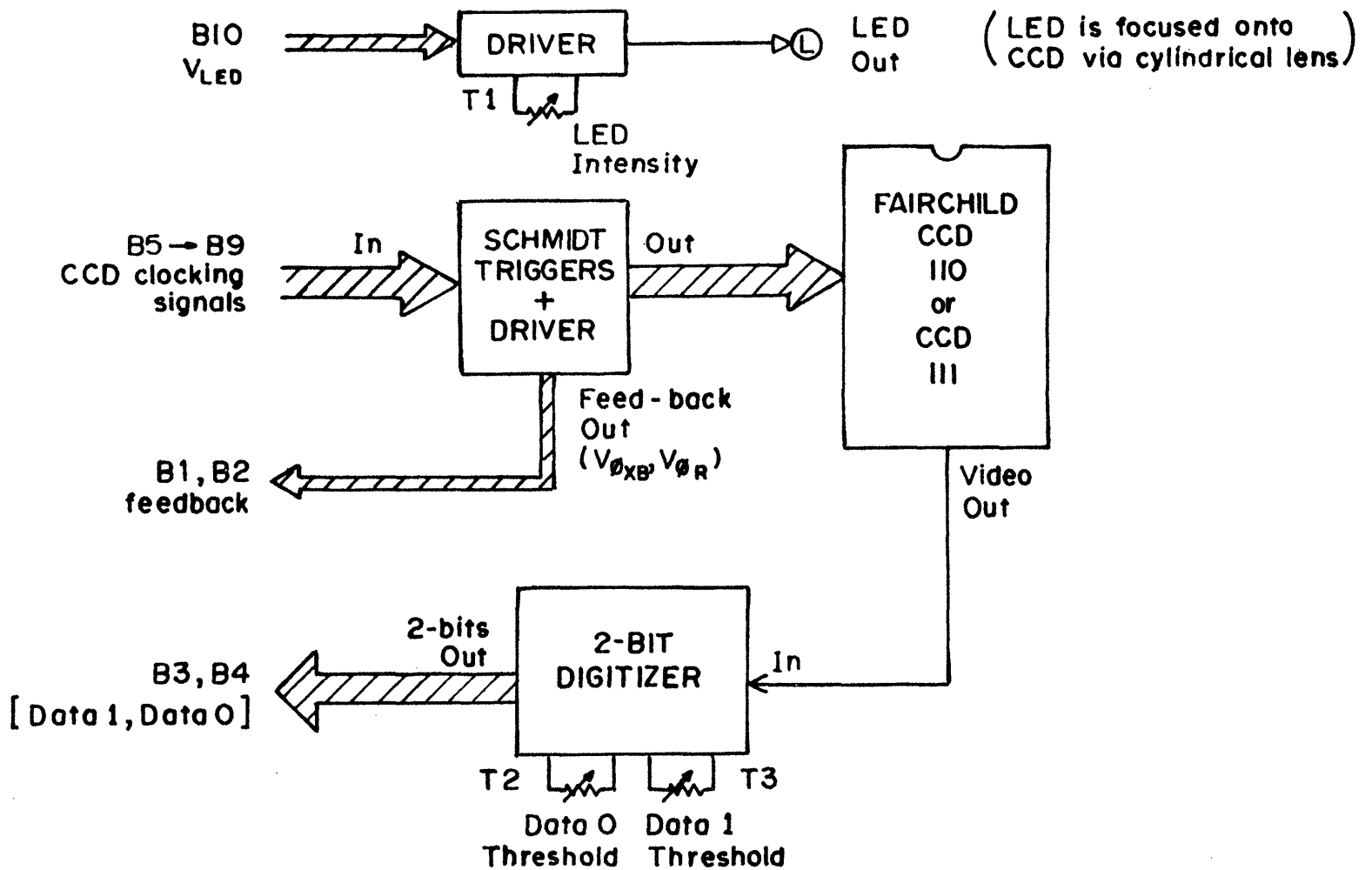
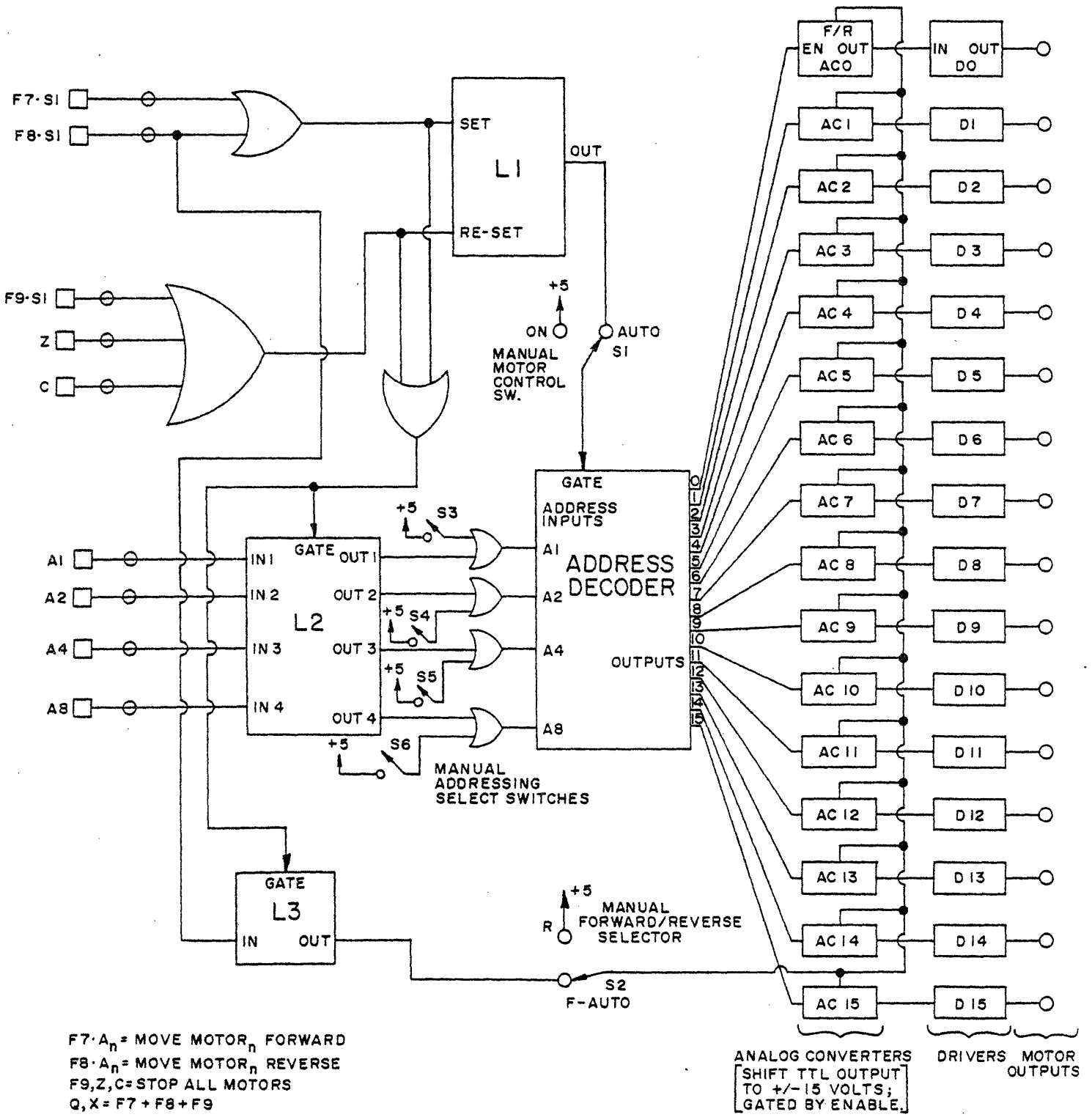


FIGURE 12

FIGURE 13

MOTOR CONTROLLER/DRIVER

BLOCK DIAGRAM



$F7 \cdot A_n$ = MOVE MOTOR$_n$ FORWARD
$F8 \cdot A_n$ = MOVE MOTOR$_n$ REVERSE
F9,Z,C = STOP ALL MOTORS
Q,X = F7 + F8 + F9

FIGURE 14

ORGANIZATION OF A PROPOSED CCD READOUT SOFTWARE SEQUENCE