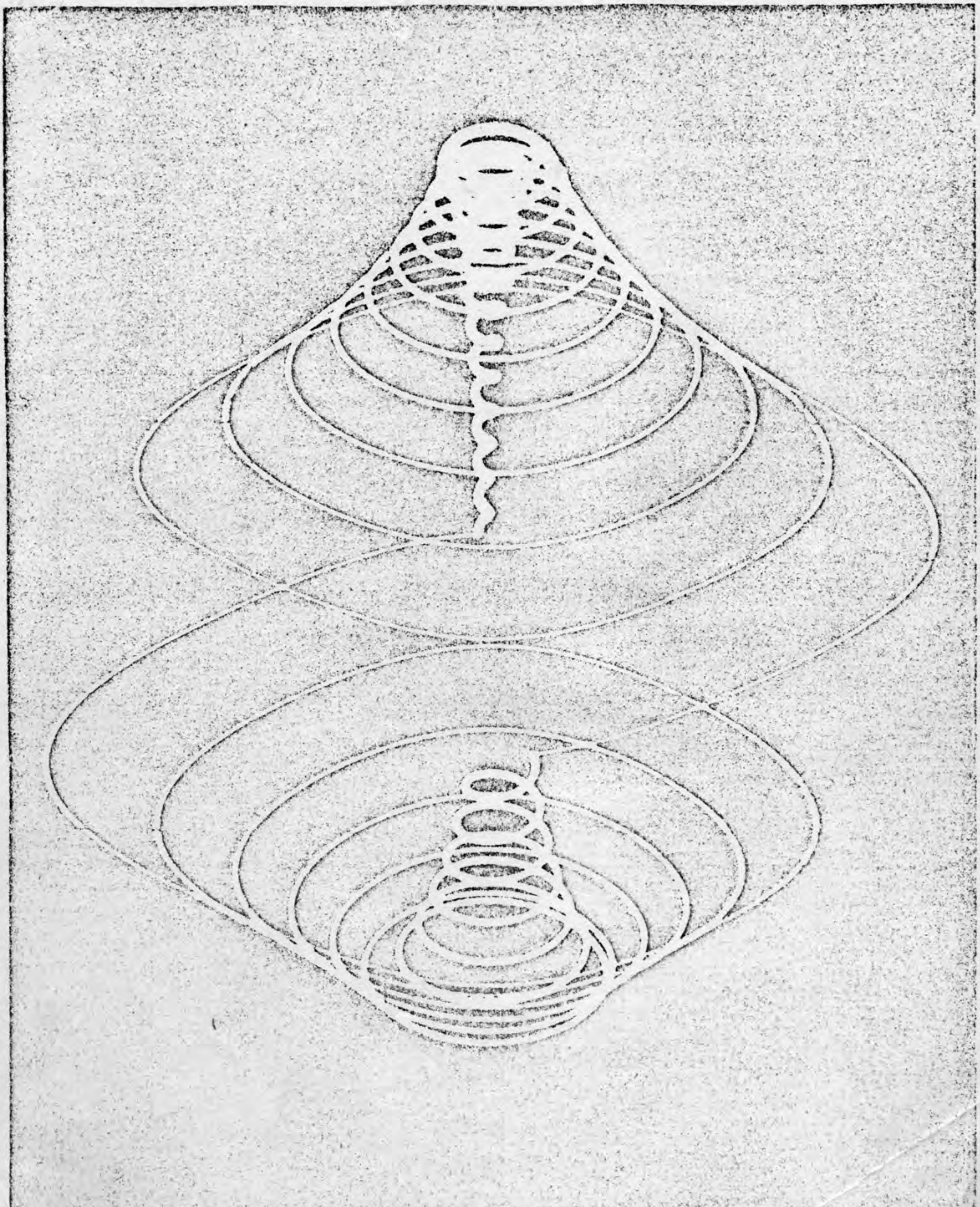
Notes on "The Design, Construction, and Operation of an Electronic Music Synthesizer"

This report was originally written to get course credit for an independent study project that I did my senior year in Electrical Engineering at Tufts University. It was written in 1977, and the device that it describes was designed and completed in the summer of 1976. It represents the first stages in my exploration of modular synthesizers. After completing my Ph.D. work in physics four years later, I found myself drawn again into designing and building synthesizer circuits during the early 80's, resulting in the realization of more than twice as many modules that are considerably more advanced. Although I have more information on my larger system posted on a website (see http://www.media.mit.edu/~joep/synth.html), I never formally documented the designs, hence this is the only readable written work on synthesizer circuits that I produced (note that my more current research directions that involve musical controllers are posted on the project site of my group: http://resenv.media.mit.edu/). In the interest of posterity and for the benefit of hobbyists, I'm posting this document publicly. Admittedly, the designs are quite primitive compared to my subsequent modules and to where electronics has evolved. But some of the circuits are still a bit interesting in a quirky way… Some of the designs were inspired by other devices, either on the market as effects boxes, or circuits published in various places that I hacked and modified – I cited all such sources in this document (in effect, it served as an undergraduate thesis of sorts). After returning to the USA following my ETH postdoc at the end of 1983, I tweaked the design of the modules in this cabinet to improve their performance and bring their spec up to the newer modules – these changes are handscrawled atop the schematics (apologies, as not all are entirely legible, although the drift is usually clear). This synthesizer still exists as documented here and works wonderfully, except for the oscillators, which I replaced during the late 80's with new designs based on the CEM 3340 VCO chips (the front panel is still the same, but the oscillator uses the Curtis chip, which is quite stable).

-- Joe Paradiso, July 2003 --



SYNTHESIZER DESCRIPTION

This was written in 1977, and served as an undergraduate "thesis". The cover photo was generated by cross-plotting low-pass vs. bandpass outputs from a state-variable filter on an oscilloscope screen.

THE DESIGN, CONSTRUCTION, AND OPERATION OF AN ELECTRONIC MUSIC SYNTHESIZER

Joseph Paradiso

ELECTRONIC MUSIC SYNTHESIZER

With the production of the first operational amplifiers in the mid 60's, it became feasible to commercially build musical instruments goverened by analog control. The manufacture and use of synthesizers has sky-rocketed after Robert Moog's initial models, and now they are very common in the music industry. Work is underway now to digitize synthesizer operation, making more breakthroughs imminent.

The music synthesizer which I have designed is basically an analog device (with some interfaced digital sections), which allows one to dynamically develop and control the pitch, timbre, and amplitude of various sound sources. It is a flexible studio-type instrument, being composed of 37 independant modules powered by a common supply. One "programs" the instrument by patching one module to another via external connections, creating the system configuration necessary to produce the desired sounds. Most sound processing modules allow one or more parameters to be varied through voltage control, with -15 volts $< V_c <$ +15 volts. Two programmable sequencers are contained in the package (one of which has psuedo-random capability), and these allow one to set control voltage patterns and step them with an external clock. Many other devices, such as the binary divider, sample holds, and LFO's aid in programming various types of control sequences internally. One can control the device by more conventional means with a three octave keyboard featuring pre-set vibrato and both linear and exponential glissando. The synthesizer is a stereo device, and sounds can be mixed dynamically through both channels by various means. There is enough equipment built into the synthesizer for several simultaneous "programs" to be running, creating the effect of a "symphony" of electronic sound.

I began researching synthesizer theory in the beginning of my Sophomore year (Sept., 1974) and I started construction several months later (March, 1975). I finished building the present hardware in July of 1976, after putting hundreds of man hours of work into the project (it is impossible to estimate any exact number). There are several more modules I am now designing that I would like to eventually add to the synthesizer.

NOTES ON CONSTRUCTION

The synthesizer is housed in a plywood cabinet measuring roughly 2.5 x 2.5 feet wide, and 1.0 foot deep. The cabined is divided into five rows. The bottom row contains the utility panel, and the remaining four house the actual electronics. The construction is completely modular, and any one unit may be easily removed for servicing. Because modules are not cross-connected internally, all patching between them must be made manually. Two sets of power supply conductors run the full lenth of the cabinet, and each module is tied to the appropriate points on this bus. All circuitry and controls are mounted on the front panels, which are made from 1/16'th inch thick aluminun plating. Most of the electronics are constructed on etched printed circuit boards. Since leads have been kept short, and voltages range high (up to +/- 15 volts), shielding is not, in general, necessary. All long audio lines are made from shielded cable, however, as an added precaution.

The conventional connector used in the synthesizer is the "test pin jack", and all patchcords used must be compatible. The utility panel provides a limited facility for interfacing with phone jacks, RCA phono plugs, and bayonet connectors.

The selection of operational amplifiers was frequently governed by the availability of devices at the time of construction. For comparators, I generally used an uncompensated 301 type, and for most low gain DC/audio applications, I found the 741 to be more than adequate. In order to conserve space on circuit boards, I often used multiple amplifier packages, such as the LM324 or the 1458. Because of its adaptability to analog circuitry, all logic used here is CMOS.

FORMAT AND CONVENTIONS USED IN THIS REPORT

This essay will be broken into thirty sections dealing independently with each module of the synthesizer. These will be generally composed of five subsections structured as follows:

I) Brief functional summary of module (With specifications where appropriate)
II) Schematic diagram
III) Technical description
IV) References
V) Illustrative waveform photographs

Most technical descriptions will refer to the diagrams. All components appearing in schematics are designated via the following alphabetic convention:

A	Operational amplifier
C	Capacitor
D	Diode (normal and zener)
LED	Light emitting diode
P	Potentiometer (mounted on front panel)
Q	Transistor (bipolar, UJT, and FET)
R	Resistor
S	Switch (mounted on front panel)
T	Trimmer potentiometer

The value or model number of each component is usually printed near its alphanumeric designation. Special-purpose components and IC's are explicitly labeled with pin diagrams. Maximum voltages are given for all electrolytic capacitors.

On most diagrams, a blue "X" indicates a point where the circuitry is external to the main board (jacks, switches, potentiometers, LED's, etc.). Some circuits require several drawings. In these cases, a block diagram is usually given, and chaining between schematics is designated by a lettered green dot and arrow.

The power-supply connections are not shown for operational amplifiers. It is assumed that they are driven by the bipolar 15 volt supply wherever possible. In the keyboard circuitry, all operational amplifiers are driven by the +/- 9 volt supply.

In many cases, Polaroid oscilloscope photographs of the various waveforms produced by particular modules are presented. The reports also include references to sources of technical information which were consulted.

NOTE: The following abbreviations will often be used in this report.

VCA	Voltage controlled amplifier (2 quadrant multiplier)
VCO	Voltage controlled oscillator
VCF	Voltage controlled filter
LFO	Low frequency oscillator

LIST OF SYNTHESIZER MODULES

No. in cabinet	Type of module
3	VCO using 8038 chip
1	VCO using UJT relaxation oscillator
2	Phase-locked Loop/VCO
1	Simple 4 input inverting summer
2	Attack/Decay transient envelope generator
1	Simple bandpass VCF
1	Simple lowpass VCF
1	Simple bandpass VCF with LFO
2	AC coupled audio VCA
1	Pulse width modulator/Sine shaper
1	Envelope follower/trigger
1	Mechanical reverberator
1	Voltage controlled "distorter"
2	Sample/Hold
2	Noise generator
1	Phase shifter
1	7 stage binary counter
1	9 stage programmable/pseudo-random sequencer
2	Transient Lag (LP filter)
1	Balanced "ring" Modulator (4 quadrant multiplier)
2	DC/AC coupled VCA
1	High range, high Q state variable VCF
1	External interface provision
1	Crest/trough diode mixer
1	Programmable 12 stage sequencer
4	Four channel mixer
2	Voltage controlled panning
1	AGC using LM370
1	Stereo output section with monitor amplifier
1	Three octave keyboard with support circuitry

1) POWER SUPPLY AND UTILITY PANEL

Power supply voltages:

Regulated (rated at one ampere maximum load)

+5 volts

-5 volts

+9 volts

-9 volts Go to ±5 +/- 15

+15 volts

-15 volts

Not Regulated (500 mA maximum load)

+18 volts

An additional 17 volt "scratch" supply is included for driving LED's and other apparatus where ripple is non-critical. This is referred to as "V_{LED}" in the diagrams.

---Power supply and Utility panel---

The +/- 15 volt supply drives most of the electronics, +/- 9 is primarily used for the keyboard, +/- 5 drives most of the logic, and +18 powers much of the transistorized circuitry. The synthesizer could be re-designed to use the +/- 15 volt supply exclusively. (The present supply developed gradually during prototype construction, and it was frequently tailored to meet the needs of specific circuitry rather than vice-versa.)

Because of its simple nature, a power supply schematic is not presented. The circuitry is quite conventional. The output of a transformer is full-wave rectified (a center-tap transformer is used for bi-polar supplies), and ripple is smoothed via large filter capacitors (10 - 50 thousand MFD computer capacitors are used). If the supply is to be regulated, the capacitor voltage is fed to integrated circuit regulators (LM390 for +5 and +9 volts, LM340 for +15 volts, LM320 for -5, -9, and -15 volts), which are mounted on heatsinks. Oscillation in supply lines is damped by placing anti-ringing capacitors in appropriate positions. The output of each supply is routed to two sets of bus wires which run the full lenth of the cabinet. A connector is provided at the rear of the synthesizer for feeding voltage to the keyboard. The +/- 15 volt supply may also be tapped via terminals mounted on the back panel.

The power supply requires standard 110 volt AC, and it is fused at 3 Amperes.

The utility panel performs several valuable functions. It contains....

The ON/OFF switch and pilot light
Six sets of 4-multiple pin jack connectors
Two sets of RCA phono plug--phone jack--bayonet connector to pin jack interfaces
Two variable +/- 5 volt DC bias sources
One variable +/- 9 volt DC bias source
Three variable attenuators (200K impedance)
Two 1N914 diodes
Three capacitors (0.01, 0.1, and 50 MFD)
Three tie points to system ground

These components can be accessed via pin jacks, and are useful in a variety of situations.

2) THREE OCTAVE KEYBOARD AND SUPPORTING CIRCUITRY

Inputs: Vibrato oscillator control (external)

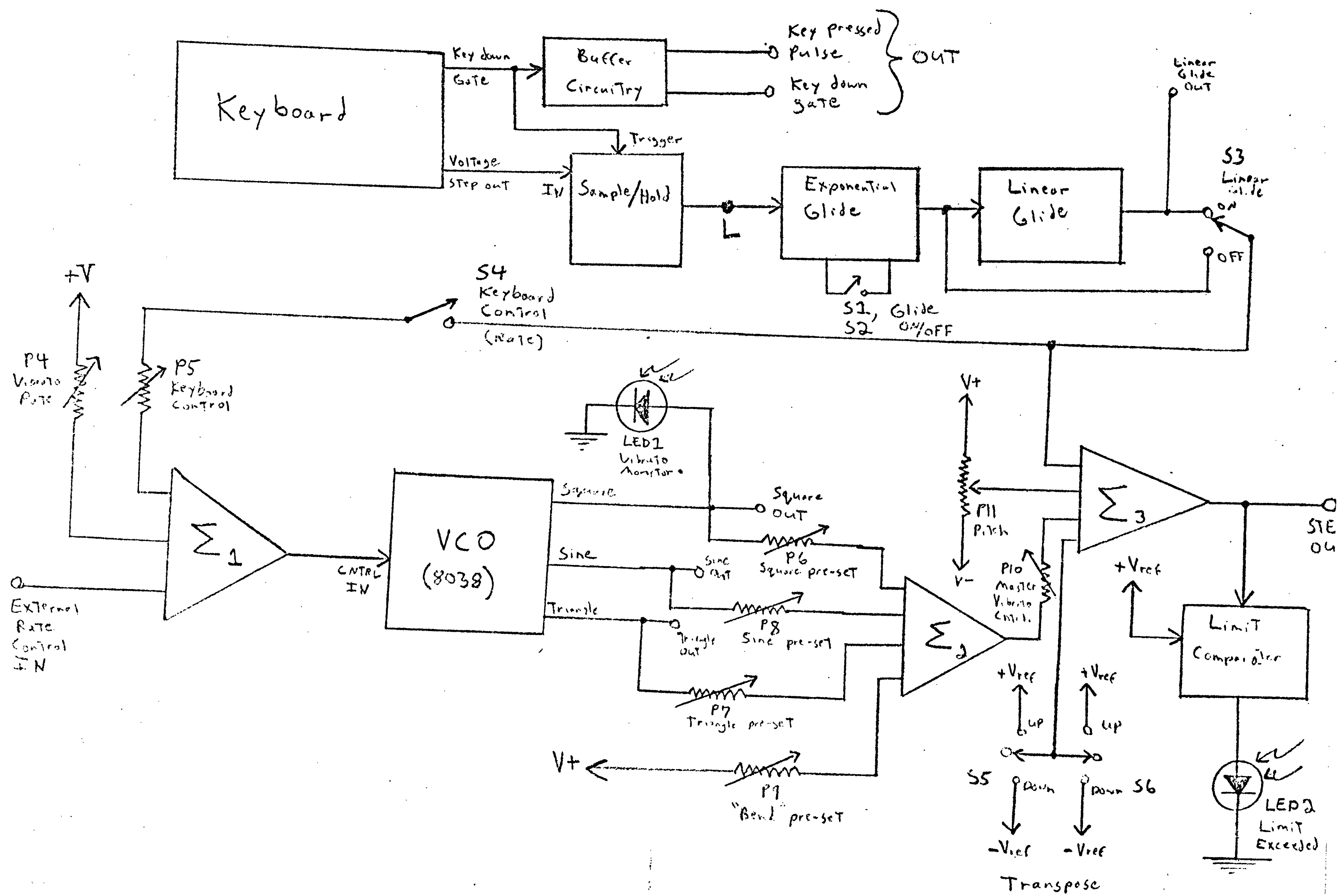
Outputs: Keyboard linear step output
"Key down" gate
"Key pressed" trigger
Vibrato oscillator sine output
Vibrato oscillator triangle output
Vibrato oscillator square output
Linear glide output

Controls: ---- 37 note keyboard (equally tempered linear steps, 1 Volt/octave)
S1 Exponential Glide (ON/OFF)
S2 Exponential Glide (pushbutton)
S3 Linear Glide (ON/OFF)
S4 Vibrato oscillator control (Internal/External)
(When on internal, the keyboard controls the oscillator's frequency
ie. high notes--fast vibrato, low notes--slow vibrato.)
S5 Keyboard transpose (Up/down)
S6 Keyboard transpose (Up/down)
P1 Exponential Glide (amount)
P2 Linear Glide attack rate
P3 Linear Glide decay rate
P4 Vibrato oscillator rate (0.4 hz - 15 hz)
P5 Vibrato oscillator internal control sensitivity
P6 Square vibrato pre-set
P7 Triangle vibrato pre-set
P8 Sine vibrato pre-set
P9 DC "bend" pre-set
P10 Vibrato/"bend" master level (mixes pre-sets into step output)
P11 Keyboard pitch

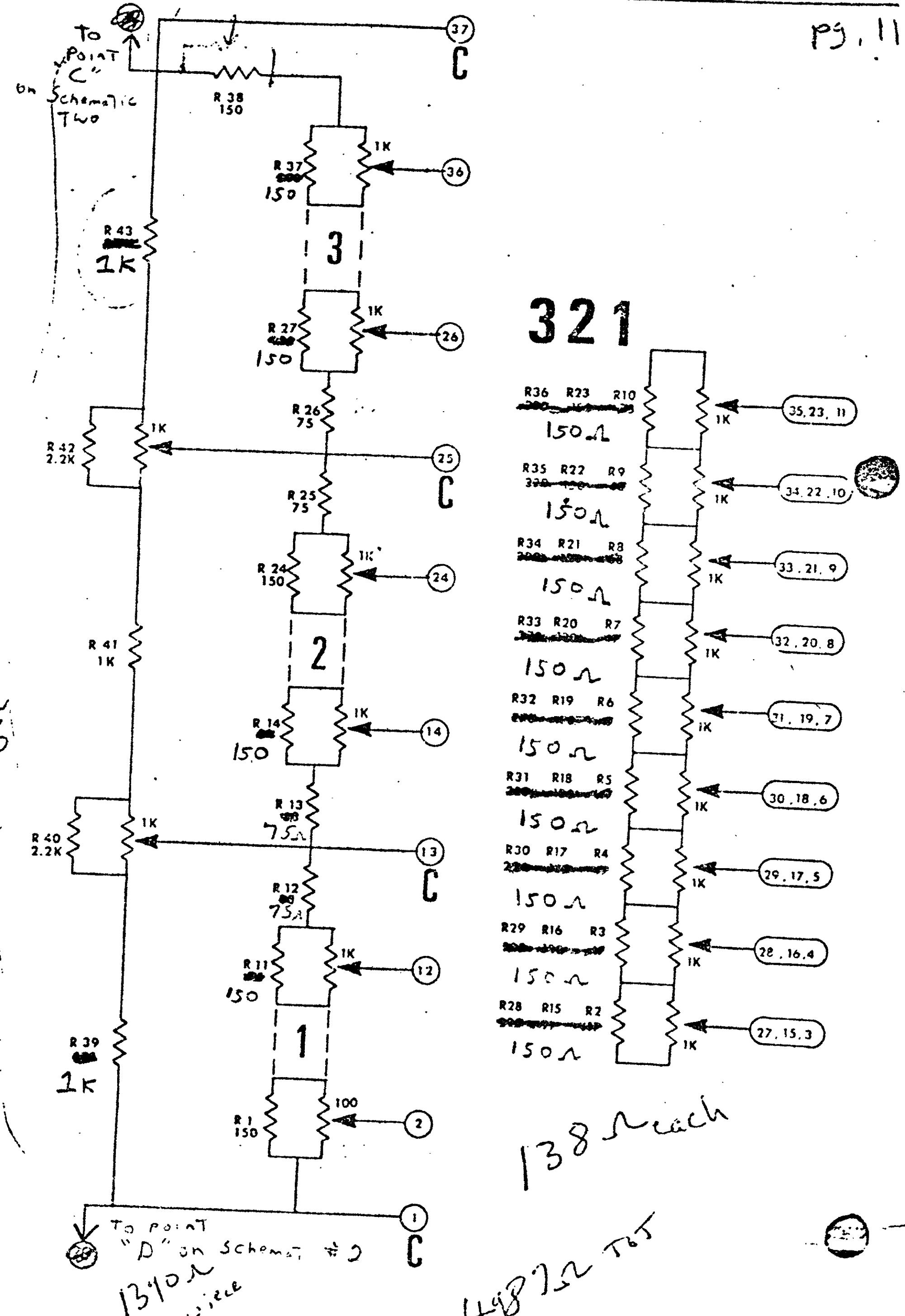
LED's: LED1 Keyboard saturation limit exceeded
LED2 Vibrato oscillator rate monitor

Uses: The keyboard is an external unit, connected to the main synthesizer power supply via an umbilical. It can be used to track exponential VCO's. One key at a time must be pressed - it is not polyphonic.

Keyboard Circuitry — Block Diagram



Schematic #1 - Keyboard Resistor Ladder



The Keyboard Taps Tie To point "E" on Schematic #2

Reduced to basics the controller is nothing more than a switch controllable voltage divider but it starts to get a little more complicated as "housekeeping" functions are added. In addition to the voltage divider the circuit includes both the current source, trigger circuit and sample/hold circuitry.

The constant current source is a standard design built around Q1 and using the voltage drop across the series combination of D1 and D2 as a reference. The output of the current source is regulated by changing the d.c. feed-back with emitter resistor R20. The current source feeds the voltage divider shown in figure 23 and represented by R_k in figure 24.

The voltage divider is implemented with a string of fixed and variable resistors as shown in figure 23. In order that the voltage output of the string be exponential, to duplicate the exponential nature of the equally tempered musical scale, the resistance values are calculated and selected so that the resistance of any parallel pair in the string is approximately 1.059 times greater than the resistance of the pair directly below it. This is further discussed in the 2720 User's Manual. In order to compensate for tolerance pile-ups over the length of the voltage divider, the trimmers for the octave points corresponding to the two middle C's of the keyboard are arranged so that they can raise and lower the voltage at those points over a 6 to 8 semi-tone spread rather than through a single semi-tone as are the other trimmers.

There are two sets of contacts associated with each key. The first set of contacts switches a voltage from the voltage divider corresponding to the key pressed and applies it to point "E" in figure 24. The second set of contacts are common to all keys and closes whenever any key is pressed. This set of contacts causes the S/H to store a new sample and also provides the step and pulse trigger outputs.

When any key is pressed it first causes the voltage pick-off switch to close, thereby applying a voltage corresponding to the position of the key to be applied to C1, which is simply an integrating capacitor to by-pass any noise that might be generated by dirt on the contacts. Next, the switch common to all keys closes, and this set of contacts does a number of things. A voltage begins to flow through the resistance string consisting of R11, R15 and R16. The current flow through R16 causes a voltage drop to appear across this resistor and this voltage is applied to the pin jack J3 where it serves as the step output. The step is differentiated by C5 and appears at pin jack J2 as the pulse output. Diode D6 serves to shunt to ground the negative pulse that would appear when the step returned to zero.

The current flow through R11 causes a voltage drop that allows current flow through R12 to turn on Q4. With Q4 on, current can flow through R13, R14, D4 and D5 to ground. This current flow raises the junction of R13 and R14 to a voltage that is high enough to insure that the Field Effect Transistor Q2 will be turned on (this FET will be covered shortly). The voltage that appears across the series string of R15 and R16 causes C4 to charge through the forward-biased D5, the significance of this will be shown presently.

The Sample and Hold circuit can further be broken down into a comparator (IC-1), a high impedance FET source follower (Q3) and a switch (Q2). The comparator is constantly comparing the input from the keyboard to the output appearing across the load resistor of the source follower (R10). The state of this comparator has no effect on the holding capacitor C2 (and consequently the output of the source follower for which this capacitor is an input) until the switch Q2 is turned on. With Q2 "on" the comparator works to make the voltages at its "+" and "-" inputs identical. When the voltages are identical the circuit is in a balanced condition.

When the key is released Q4 turns off which removes the current flow through D4 and D5. Simultaneously, the positive side of C4 is allowed to go to ground through R15 and R16. In this configuration the negative side of C4 is connected to C10 through D4 and D4 is forward biased for these conditions, the charge that was on C4 now "dumps" onto C10 and since the positive side of C4 is at ground, the ungrounded end of C10 is pushed about 15 volts negative with respect to ground. This high negative voltage is applied to the gate of Q2 thereby turning this FET off. All possible leakage paths for the voltage across C10 are at this point either reverse biased diodes, "off" transistors, or the reverse biased gate junction of Q2. Since there is no discharge path for C10 its voltage remains high and holds Q2 off for an extended period of time.

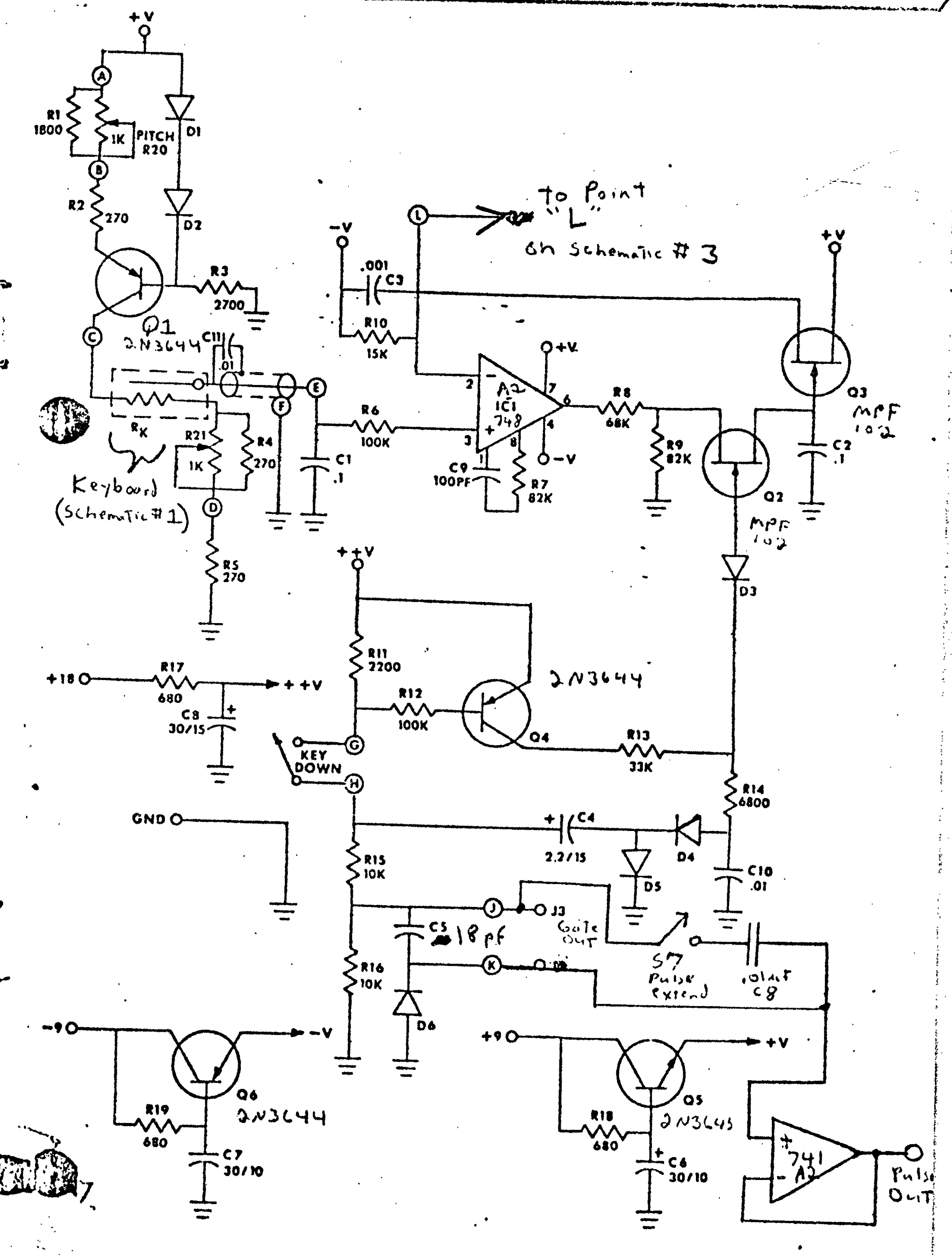
With Q2 off, the holding capacitor C2 is isolated from any discharge paths but the voltage across this capacitor still serves as the input for the source follower so the output voltage at point "L" does not change.

Q5 and Q6 serve as capacitance multipliers for the filter capacitors C6 and C7.

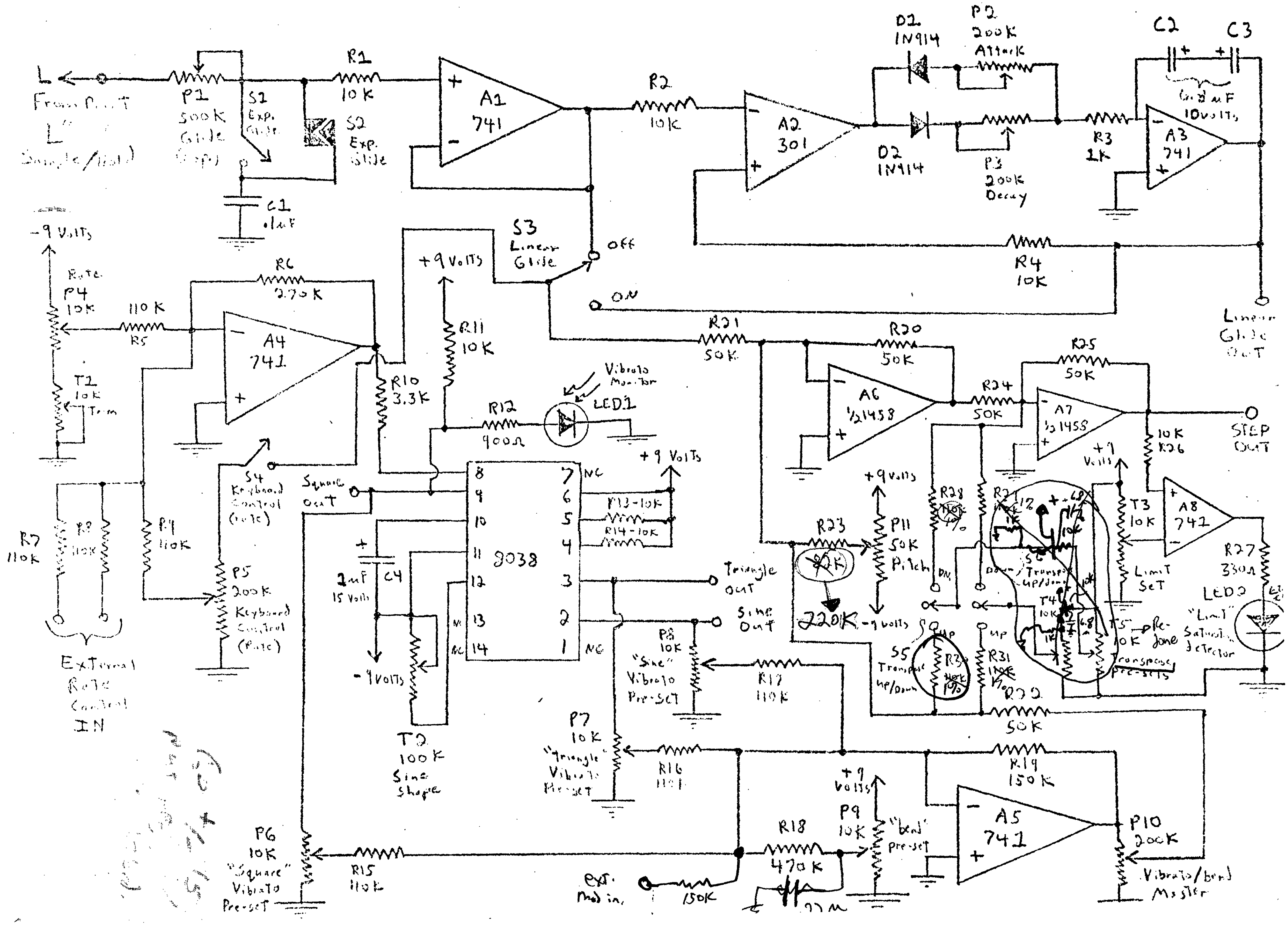
S1 and C8 were added To "extend" The decay of The pulse output, The 741 was added to buffer The pulse.

pg. 12

Schematic #2 - Sample/Hold and Buffer Circuitry



Keyboard Support Circuitry - Schematic #3 pg. 13



---Keyboard and support circuitry---

The block diagram displays the configuration of keyboard circuitry. Whenever a key is pressed, the "Key down" gate goes high. This voltage is buffered to yield the "Key down gate" output and differentiated to yield the "Key pressed pulse" output. The keyboard also outputs a voltage step (proportional to the key pressed -- 1 volt/octave), which is input to a sample/hold. When a key is down, the S/H samples the keyboard output, and it holds when the key is released. Thus at poi "L" we always have a voltage proportional to the last key pressed.

This voltage is fed through two circuits which can add an optional linear or exponential slew. It is then summed in Summer#3 with the transpose switch outputs, vibrato/bend output, and "Pitch" offset to yield the final "Step output". A comparator monitors this output, and activates a warning LED whenever the keyboard output is saturated at its positive limit.

Summer#1 adds the External Rate control voltage, the rate offset, and an optionally weighted output from the keyboard. The output of Summer#1 controls the frequency of the vibrato oscillator. The square, sine, and triangle outputs of this oscillator are wieghted through "Pre-sets" P6, P7, and P8, and added in Summer#2 with a DC bend from P9 to produce the type of vibrato wave desired. The output of Summer#2 is fed to Summer#3 via the master attenuator P10, where it is added to the keyboard output.

Schematic#1 shows the resistance ladder employed to generate the voltage steps. In the original design, the resistors were arranged to yield exponential steps, but I have made modifications to yield a linear (wrt. key pressed) output.

Looking at Schematic#2, we see that the keyboard is fed from current source Q1. The voltage picked off is input to the Sample/Hold A1, Q2, and Q3, where C2 is the hold capacitor "trapped" between the two FET's. (Since the FET's are incorporated into the feedback loop of A1, they are linearized.) When a key is pressed, Q2 is turned on via Q4, and the S/H is in "sample" mode. When the key is released, a negative charge is dumped onto C10 from C4, turning Q2 off and putting the S/H into "hold" mode. The "key down" gate is differentiated via C5 (or C8), and buffered through voltage follower A2, appearing as the "Pulse output".

The output of the S/H is fed to the keyboard support circuitry on Schematic#3. The RC lowpass filter composed of P1 and C1 adds a transient response to the signal (Provided C1 is switched in), and this is buffered in A1, giving us our "exponential glide". The linear glide circuit is composed from comparitor A2 and integrator A3.

A2 charges A3 until the output of the integrator is made equal to the input of the comparator. This results in a linear ramp at the output of A3 in response to a change in input-- ie. our desired linear slew. The rate at which integrator A3 charges is determined from P2 and P3, which, because of diodes D1 and D2, allow us to set independent "rise" and "fall" times for our ramp.

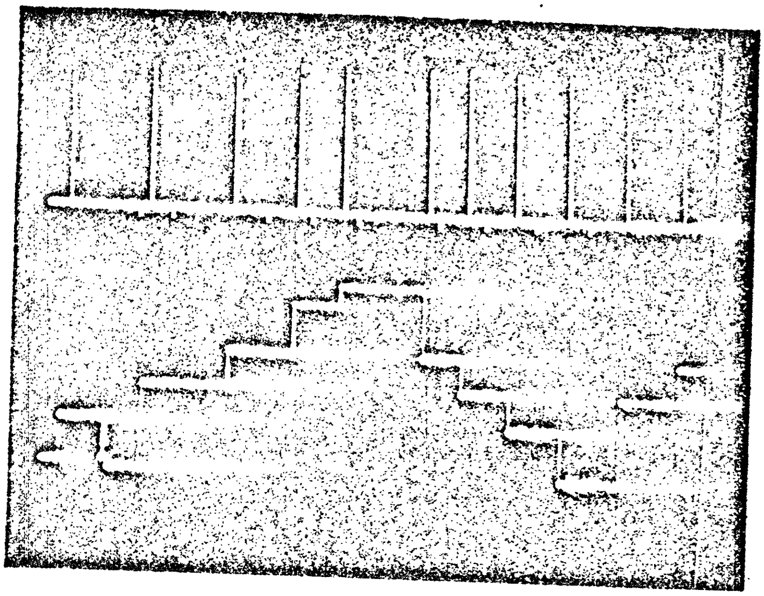
The remainder of the circuitry in Schematic#3 was discussed quite throughly while describing the block diagram. A4 is summer#1, the VCO is the 8038 chip, A5 is summer#2, A6 and A7 form summer#3, and A8 is the limit comparator.

References:

Keyboard Sample/Hold network - Paia Electronics

8038 data - Intersil application notes

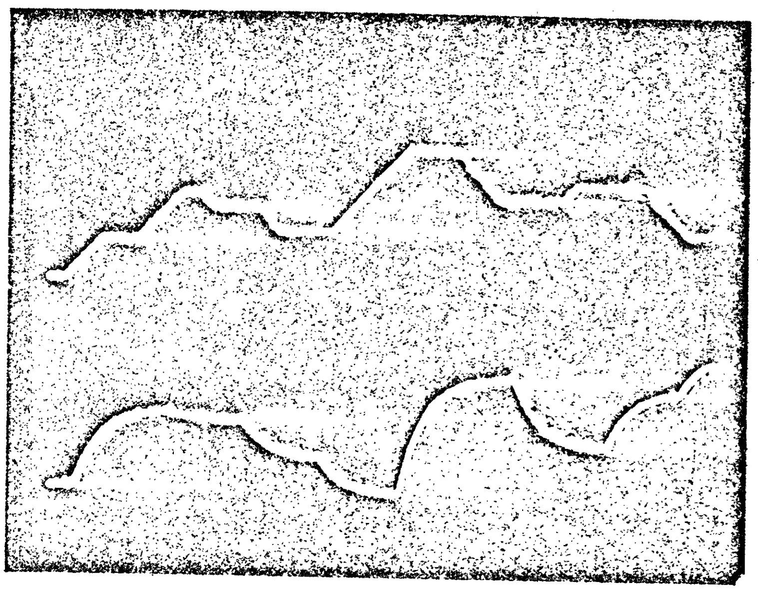
---Keyboard and support circuitry---



Keyboard "key pressed" pulse output

Keyboard step output

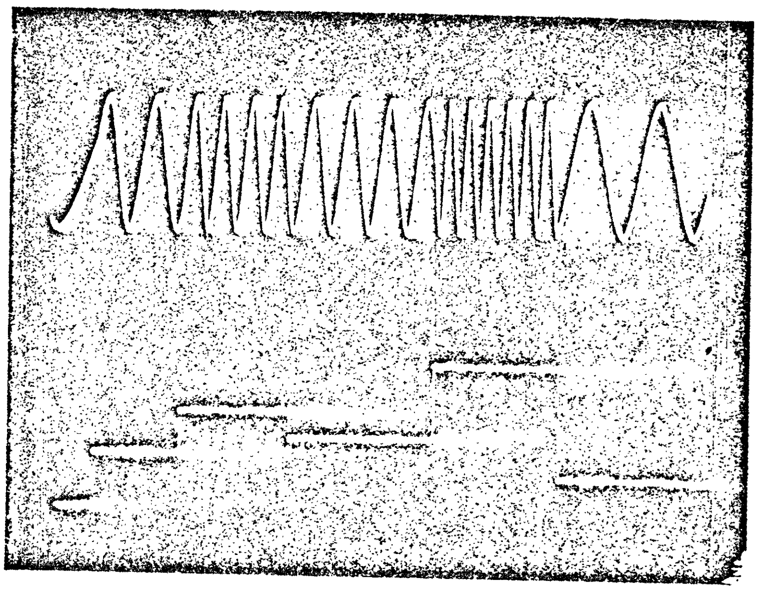
Photo#1 - step and pulse response seen while playing keyboard.



Keyboard step output with linear glide

Keyboard step output with exponential glide

Photo#2 - step outputs with linear and exponential glide



Vibrato osc. sine output

Keyboard step output

Photo#3 - Vibrato oscillator frequency vs. keyboard step output with vibrato osc. controlled internally.

3) VOLTAGE CONTROLLED OSCILLATOR

Range: Using 8038 chip... (in 5 ranges)

- 0.022 hz - 1.3 hz
- 2.6 hz - 52 hz
- 21 hz - 851 hz
- 185 hz - 7,023 hz
- 1,112 hz - 37,345 hz

Using UJT relaxation oscillator... (in 4 ranges)

- 0.01 hz - 0.3 hz
- 0.5 hz - 55 hz
- 10 hz - 1,364 hz
- 278 hz - 23,370 hz

Inputs: Exponential control scaled 1 volt/octave

Variable +/- exponential control

Linear control

Pulse width modulation

Synchronization (multivibrator re-set)

Outputs: 8038 chip...

- Sine - 4 volts p-p
- Triangle - 4 volts p-p
- Square - 18 volts p-p
- Pulse - 0-4 volts

UJT oscillator...

- Ramp - 0-3.5 volts
- Triangle - 0-2.5 volts
- Pulse - 0-5 volts

Mix: Sine, triangle, pulse on 8038

Ramp, triangle, pulse on UJT

Exponential control voltage out

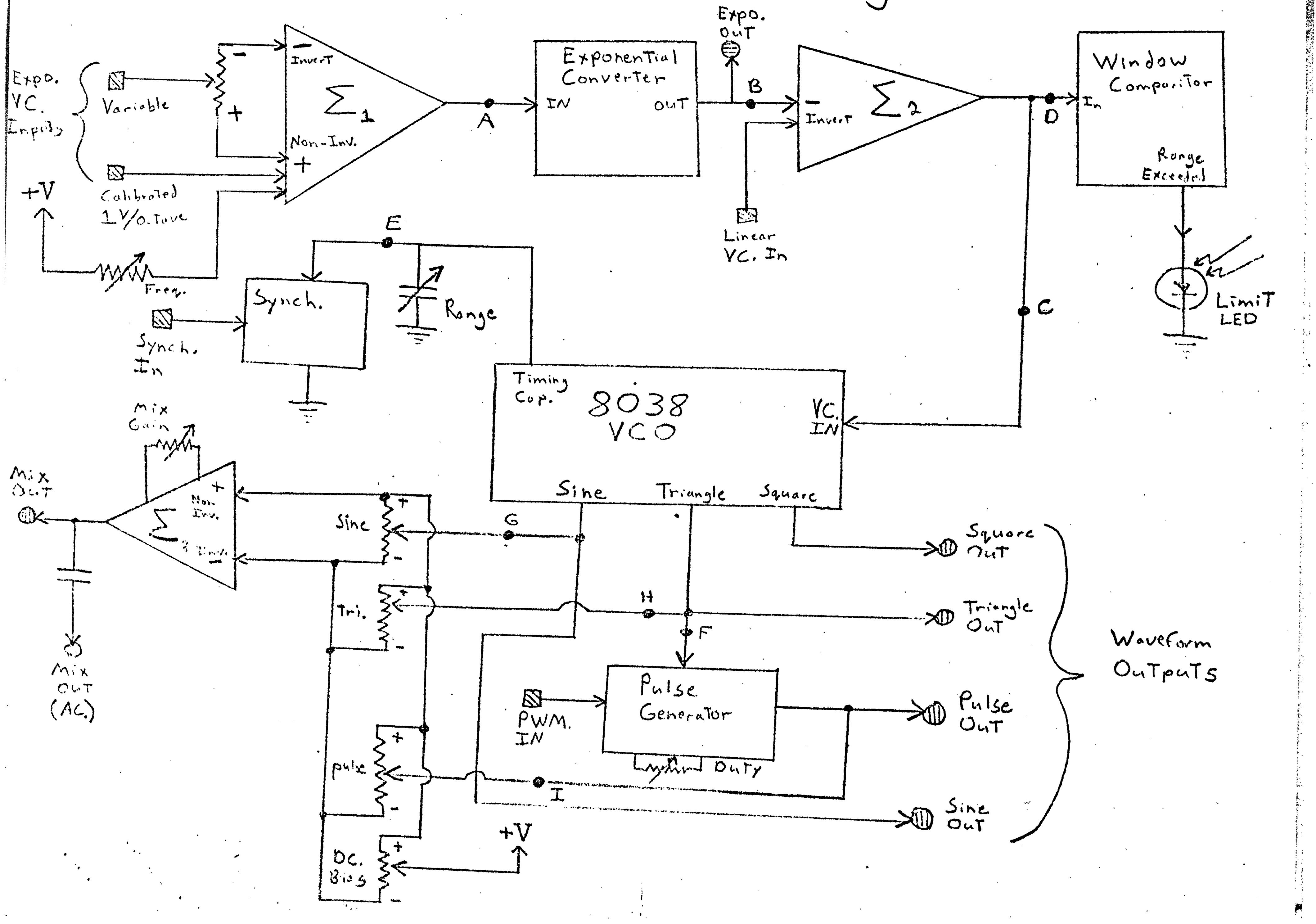
Controls:	S1	Frequency range
	S2	Frequency range
	P1	Fine frequency adjust
	P2	Coarse frequency adjust
	P3	Variable exponential control (+/-)
	P4	Pulse width (0-100%)
	P5	Sine mix level (+/-) (ramp on UJT)
	P6	Triangle mix level (+/-)
	P7	Pulse mix level (+/-)
	P8	DC bias in mix (+/-)
	P9	Master mix gain control

LED's LED1 Control voltage exceeds limits -- oscillator saturated

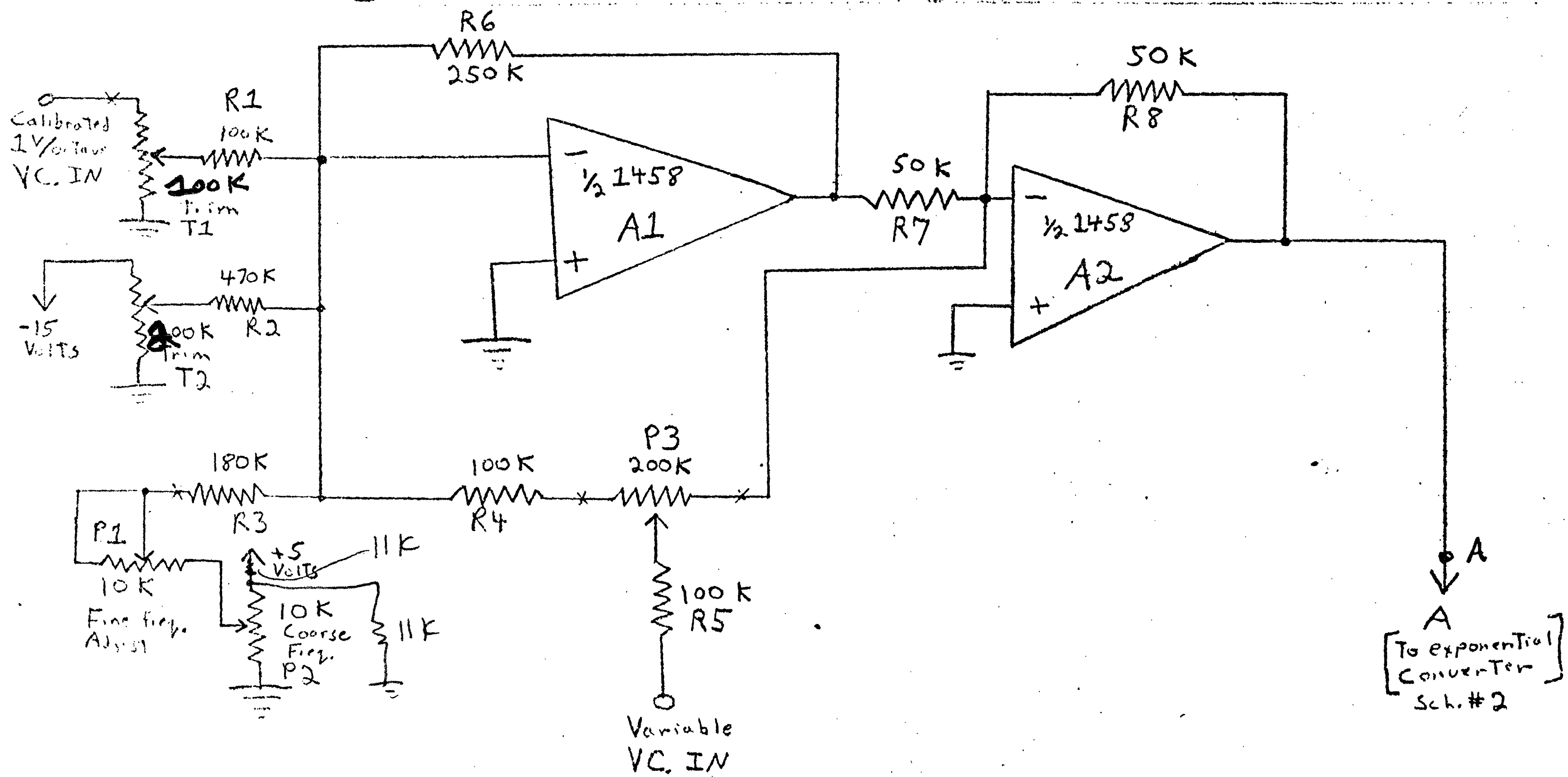
Uses: Primary tone generator in synthesizer, tracks with keyboard. Can also be used for control as an LFO.

VCO Block Diagram

pg. 20

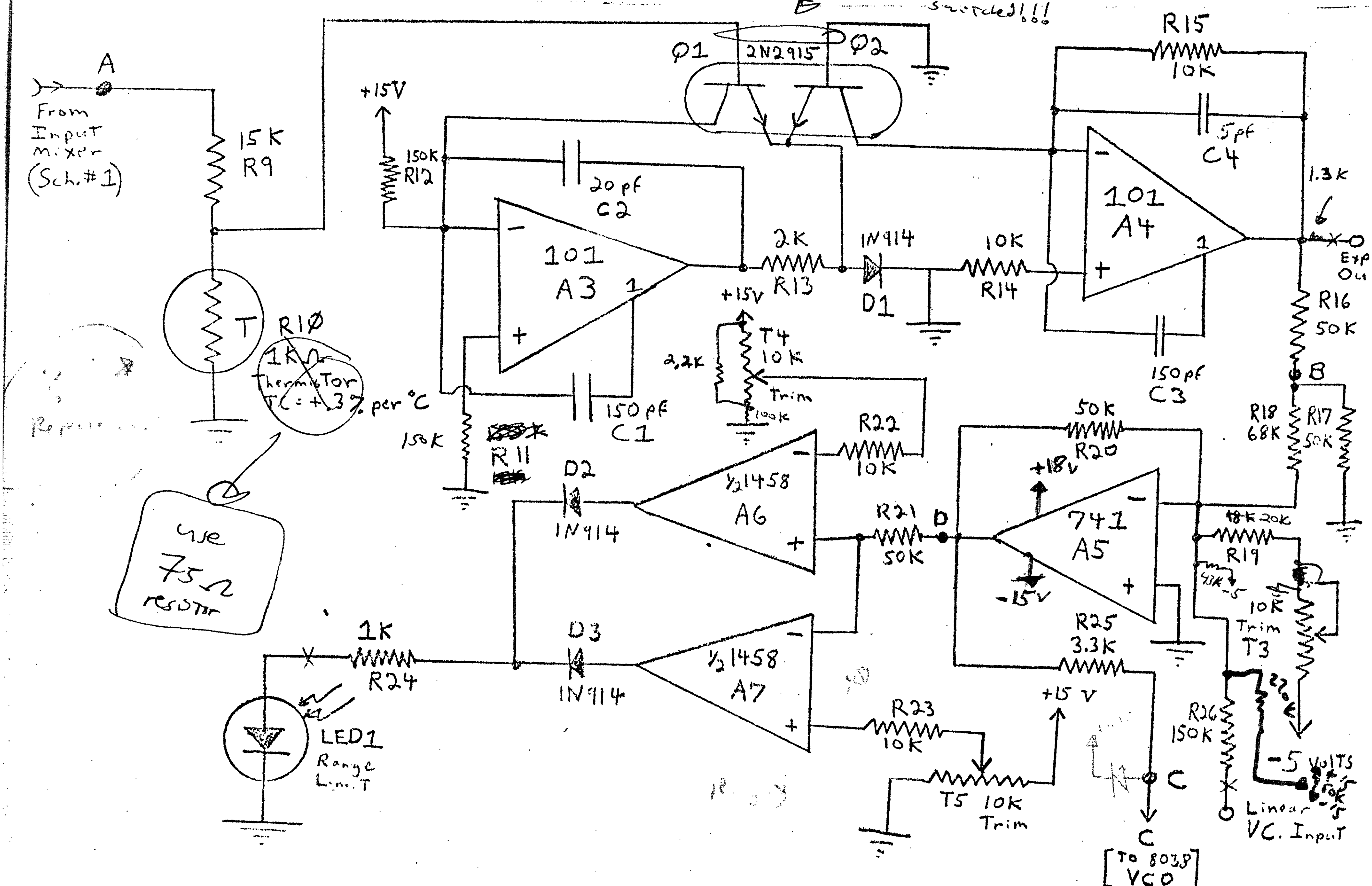


VCO Schematic #1

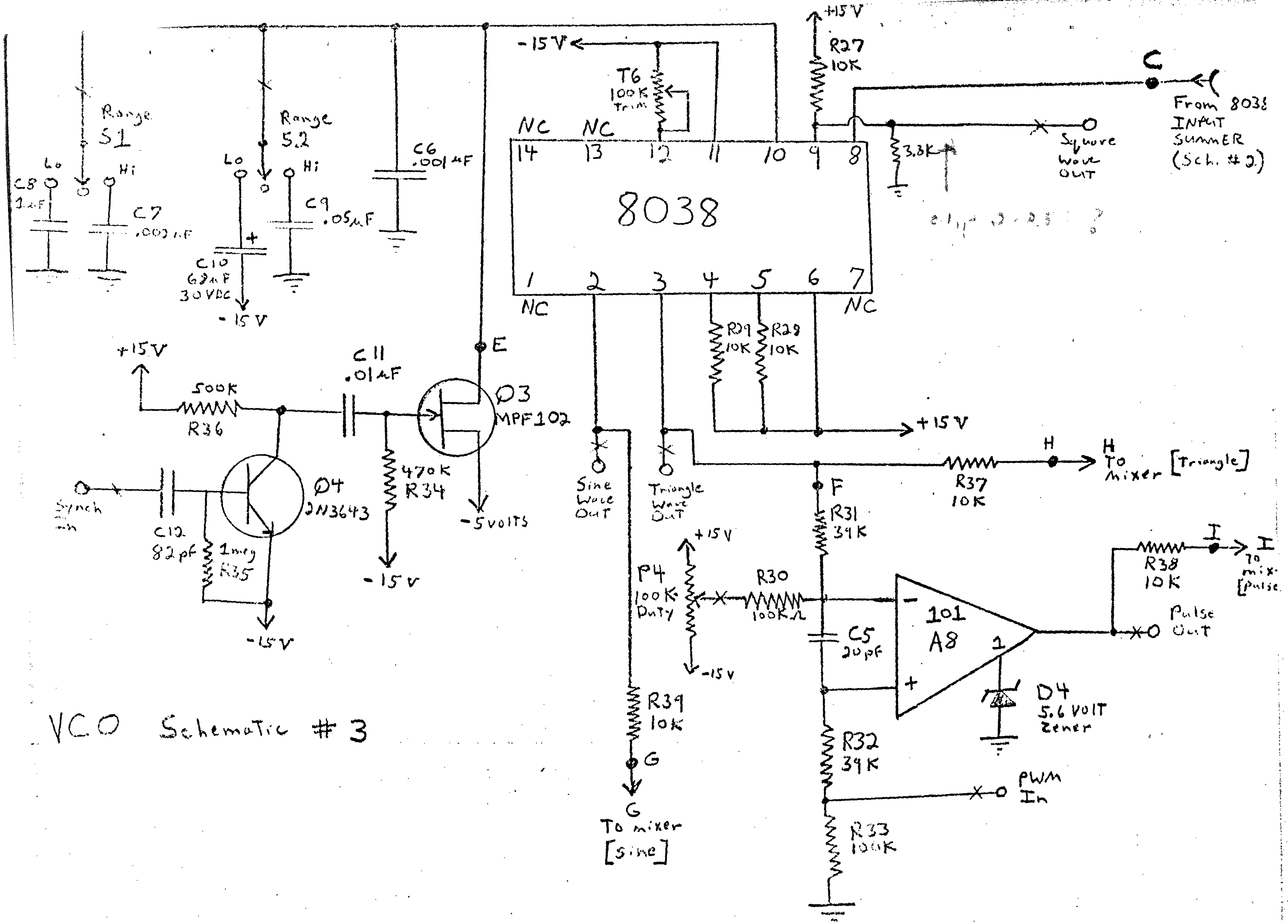


Frequency Control Input Mixer

VCO Schematic #2



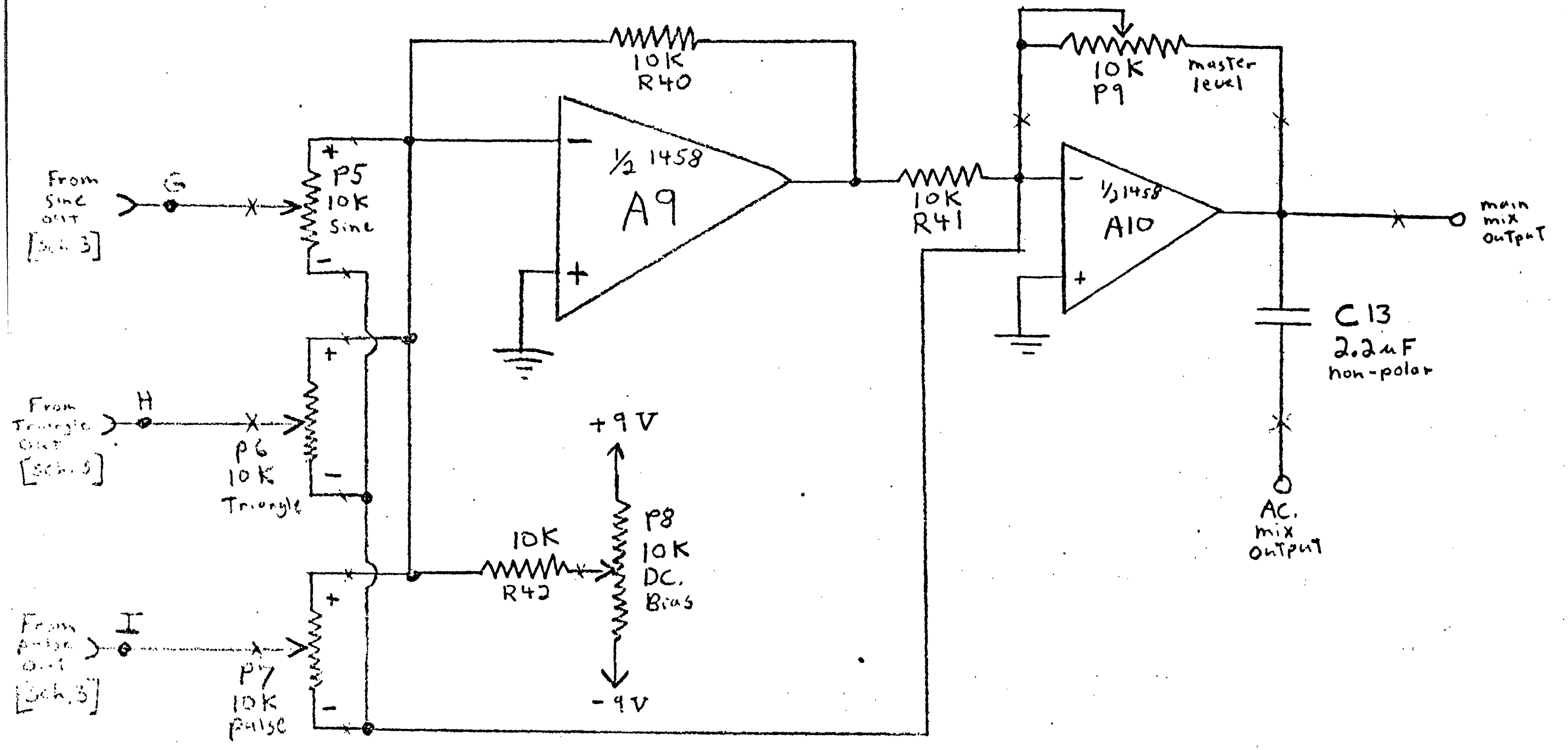
Exponential Converter, 8038 Input Summer, and Window Comparitor



VCO Schematic #3

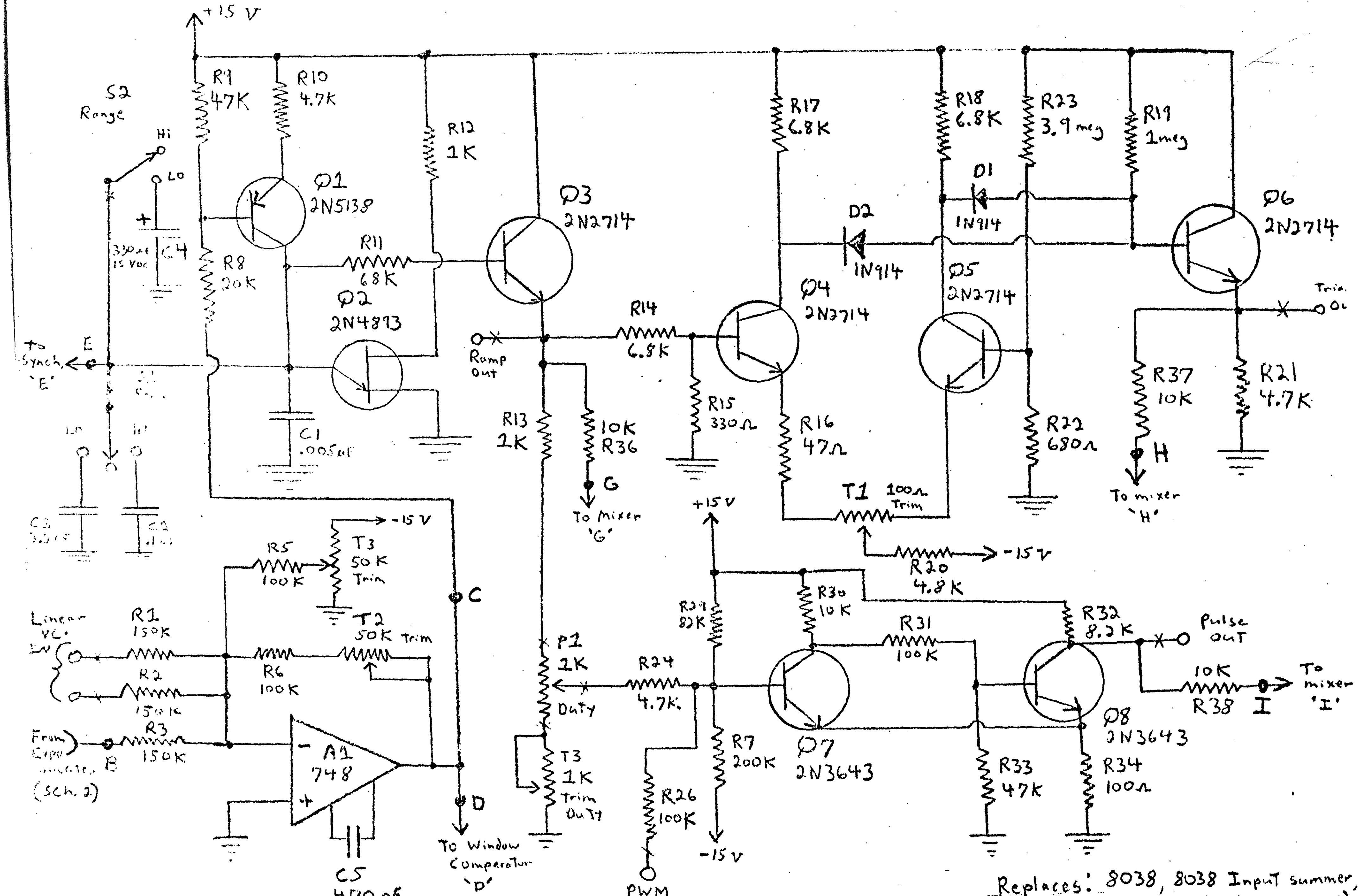
8038 master oscillator, Pulse generator, and Synchronizer

VCO Schematic #4



Output mixer

VCO Schematic #5



Alternate Oscillator

Replaces: 8038, 8038 Input summer

---Voltage Controlled Oscillator---

We can observe the structure of the VCO circuit from the block diagram. Control voltages are summed with a bias determining the "rest" frequency in summer#1. This sum is fed into the exponential converter (Volts out = exp(volts in)) then inverted and added to the linear control input by summer#2. The output of summer#2 is used as the control voltage for the 8038 and is monitored by the window comparator which activates a warning LED when out of range. The 8038 outputs sine, triangle, and square waves. A comparator has been added to the triangle wave to produce a duty-variable pulse. A synchronization circuit allows one to re-set the waveforms in synch with a controlling signal. Summer#3 mixes the sine, triangle, and pulse signals together with an optional DC bias to produce complex waveforms.

Schematic#1 shows summer#1. T2 is adjusted to give a negative bias to the output, allowing us a 28 volt (roughly) range from -14 to +14 volts. T1 is adjusted so that the calibrated control input is set to 1 volt/octave. P1 and P2 add bias, allowing us to set our "rest" frequency. P3 lets us route an input to eith A1 or A2, enabling both "straight" mix and inversion.

The output of summer#2 is scaled by a temperature-compensated voltage divider (R9, R10) and fed to the base of Q1. A3 maintains the collector current of Q1 constant, setting the voltage at the emitter of Q2 such that the collector current of Q1 is exponentially related to our input voltage at the base of Q1. A4 is a current-to-voltage converter which converts Q2's collector current into an output voltage. (Both A3 and A4 are feed-forward compensated via C1 and C3 for speed optimization.)

This "exponential" output voltage is summed with the "linear" control input and a bias set by T3 in A5, where it is inverted and routed to the input of the 8038. (T3 is adjusted to align the exponential output with the frequency of the VCO. We have the general equation: Frequency = exp(k1*Vin) + k2. T1 sets k1 and T3 sets k2.) A6 and A7 form a window comparator which activates LED1 when this control voltage is out of range. (The upper trip point is set by T4, and the lower trip point is set by T5).

S1 and S2 allow us to switch-select the timing capacitors employed by the 8038, giving us control over the range of the oscillator. Q4 is an amplifier which buffers and differentiates the "synch" input. Whenever Q4 switches off,

---Voltage Controlled Oscillator---

a pulse is sent through C11, turning FET Q3 momentarily on. Since Q3 shunts the timing capacitor, it is effectively discharged, and the 8038 waveform is re-set. R34 provides a negative bias on the gate of Q3, keeping it normally off.

A8 is a comparator which compares the sum of the triangle wave plus a bias voltage set through P4 against the voltage at its '+' terminal. If the "PWM" input is not connected, this '+' voltage is grounded through R33. Thus P4 will control the point at which the triangle wave at A8's '-' input crosses ground, controlling the duty of the rectangular wave at the comparator's output. A signal applied to the "PWM" input will alter the voltage at A8's '+' terminal, allowing us linear control over pulse width. Zener diode D4 clamps the pulse output ot A8 positive, and limits its maximum to roughly 5 volts.

P5, P6, and P7 route the sine, triangle, and pulse outputs respectively to either A9 or A10, allowing us to mix these waveforms with inversion capability. P8 adds a desired DC bias into the mix.

There are three 8038 VCO's in the synthesizer. Another VCO has been built, however, which does not use the 8038, but employs a discrete UJT relaxation oscillat instead. All input and support circuitry is similar to the 8038 case. Schematic#5 depicts thic new oscillator and labels the points at which it is tied into the other diagrams.

A1 here mixes the exponential and linear control voltages with a bias set from T3, performing a similar function to A5 in schematic#2. This inverted mix is fed into the base of Q1, controlling its collector current, thus controlling the rate of charge of timing capacitor C1 (C2, C3, and C4 are also switch-selectable through S1 and S2). This capacitor will charge until it reaches the trigger voltage of UJT Q2. At this point, Q2 turns on and discharges C1, allowing it to charge up again after it drops below Q2's holding voltage. Thus the voltage across C1 forms a linear ramp wave, which is buffered through emitter follower Q3 and output.

The ramp wave from Q3 is fed into differential pair Q4 and Q5. The original signal at the collector of Q5 is mixed with its inversion at the collector of Q4 through diodes D1 and D2. Because of the diodes, whichever voltage (at Q4 or Q5) is less appears at the base of Q6. This will form a triangle wave from our original ramp. (Because of the finite recovery time of the ramp wave, a small "glitch" can be seen at the apex of triangle waves shaped via this method.) Q6 is an emitter follower which buffers the triangle wave before it is output.

The ramp wave is also fed via P1 to the comparator composed of Q7 and Q8. This produces a pulse whose duty cycle is controlled by P1. The bias on Q7 can be altered by applying a voltage at the "PWM" input. This moves the comparator's trip points and modulates the duty cycle of the pulse.

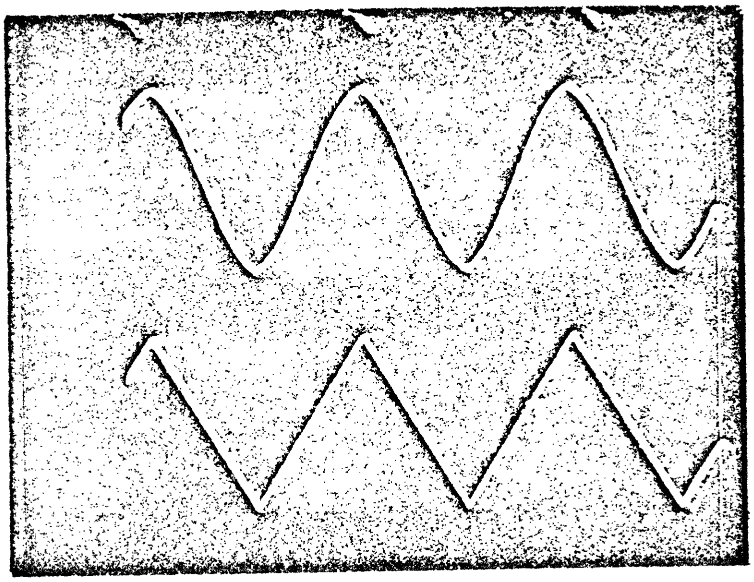
Because of the non-linearity of the 8038 and UJT oscillators, and because of inaccuracies in the exponential converter, this oscillator can be kept in tune over a fairly small (approx. 3 octave) range. I am now in the process of constructi superior oscillators using Operational Ttansconductance Amplifiers (CA3080), which are much more linear, have a greater range, and require a much simpler exponential converter design.

References:

Exponential converter - IC OP-AMP Cookbook by Walter K. Jung, Sam's Publication page 214

UJT Oscillator - Modified original design proposed by PAIA Electronics

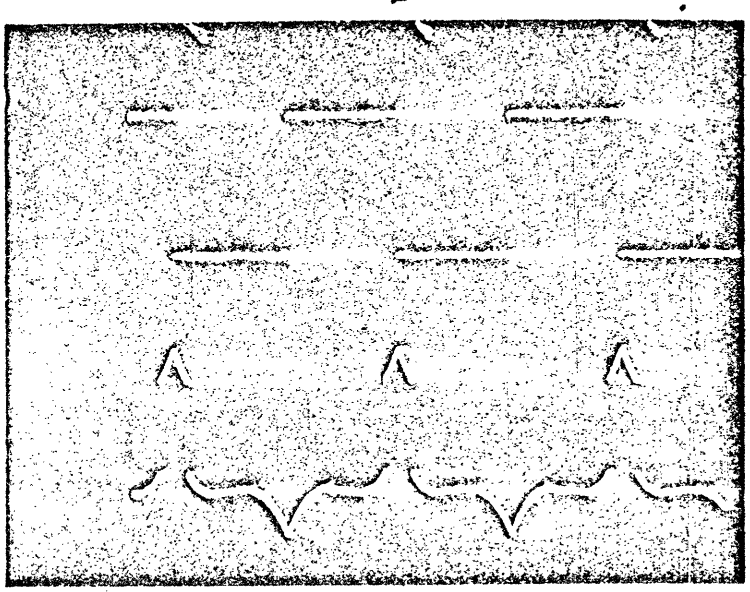
8038 Data - Intersil application notes



Sine wave output

Triangle wave output

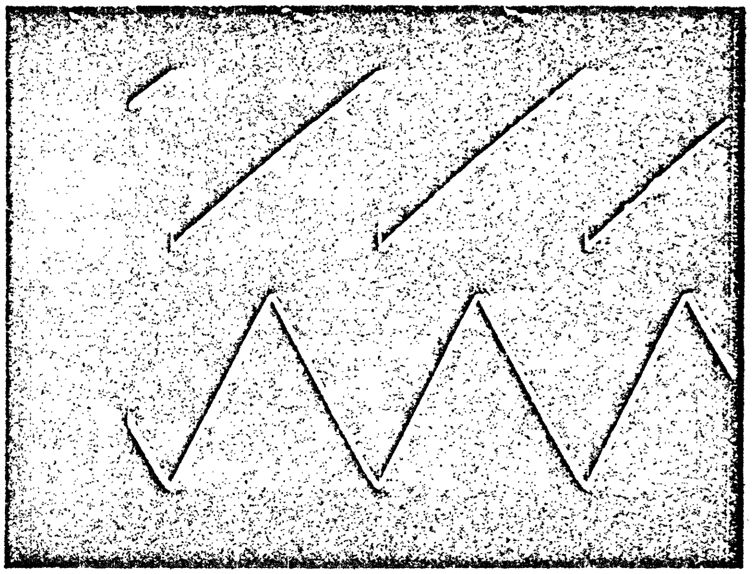
Photo#4 - 8038 waveforms



Square wave output

Complex waveform made from mixing the sine, triangle, and pulse

Photo#5 - 8038 waveforms



Ramp waveform

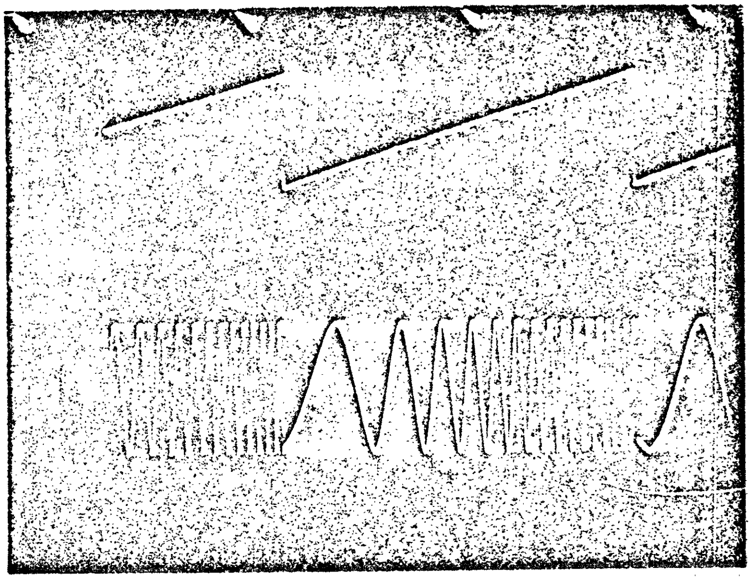
Triangle waveform

Photo#6 - UJT oscillator waveforms

Linear ramp input to exponential converter

Output of exponential converter

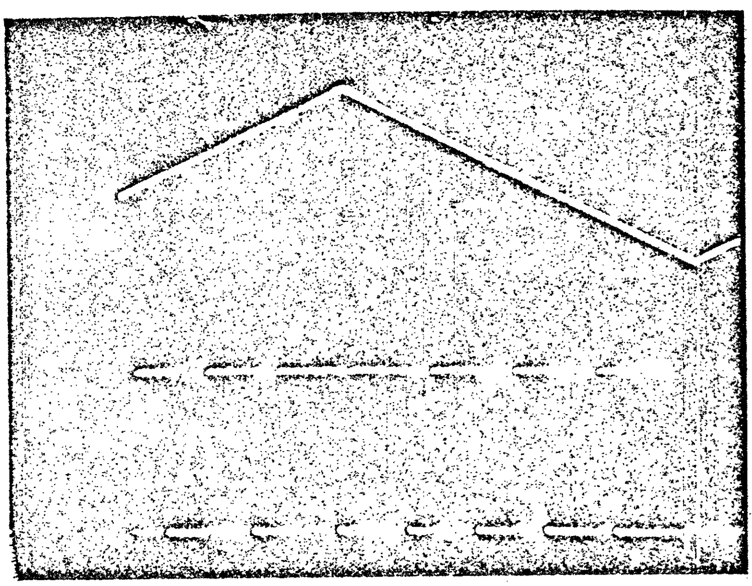
Photo#7 - Exponential converter transfer function



Linear ramp input to exponential VCO input

sine output of VCO

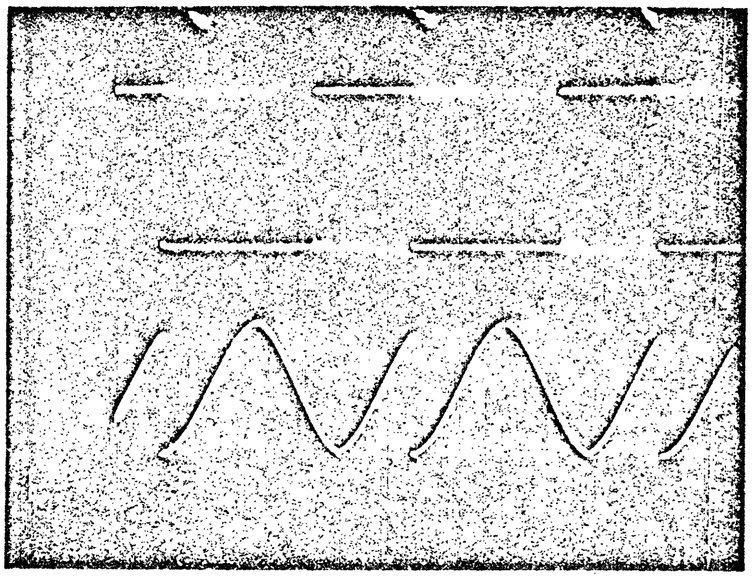
Photo#8 - Control voltage vs. output of VCO



Signal applied to PWM input

Pulse output

Photo#9 - Pulse width modulation



Pulse input to synchronizer

Synchronized sine wave

Photo#10 - Synchronization of VCO by pulse

4) PHASE-LOCKED LOOP/VCO

Range: Lock ranges...
- 16 hz - 1,980 hz (S5 Low)
- 16 hz - 3,140 hz (S5 High)

VCO Ranges...
- 16 hz - 1,950 hz (S5 low, S2 off)
- 16 hz - 3,010 hz (S5 high, S2 off)
- 1 hz - 25 hz (S5 low, S2 on)
- 1 hz - 42 hz (S5 high, S2 on)

Inputs:
- Tracking frequency input
- External phase comparator input
- External error input
- Fixed oscillator control input (linear)
- Variable (+/-) oscillator control input (linear)
- Disable input (shuts down micro-power circuit)

Outputs:
- Oscillator output (Square wave 0-4 volts)
- Error output
- Demodulated output

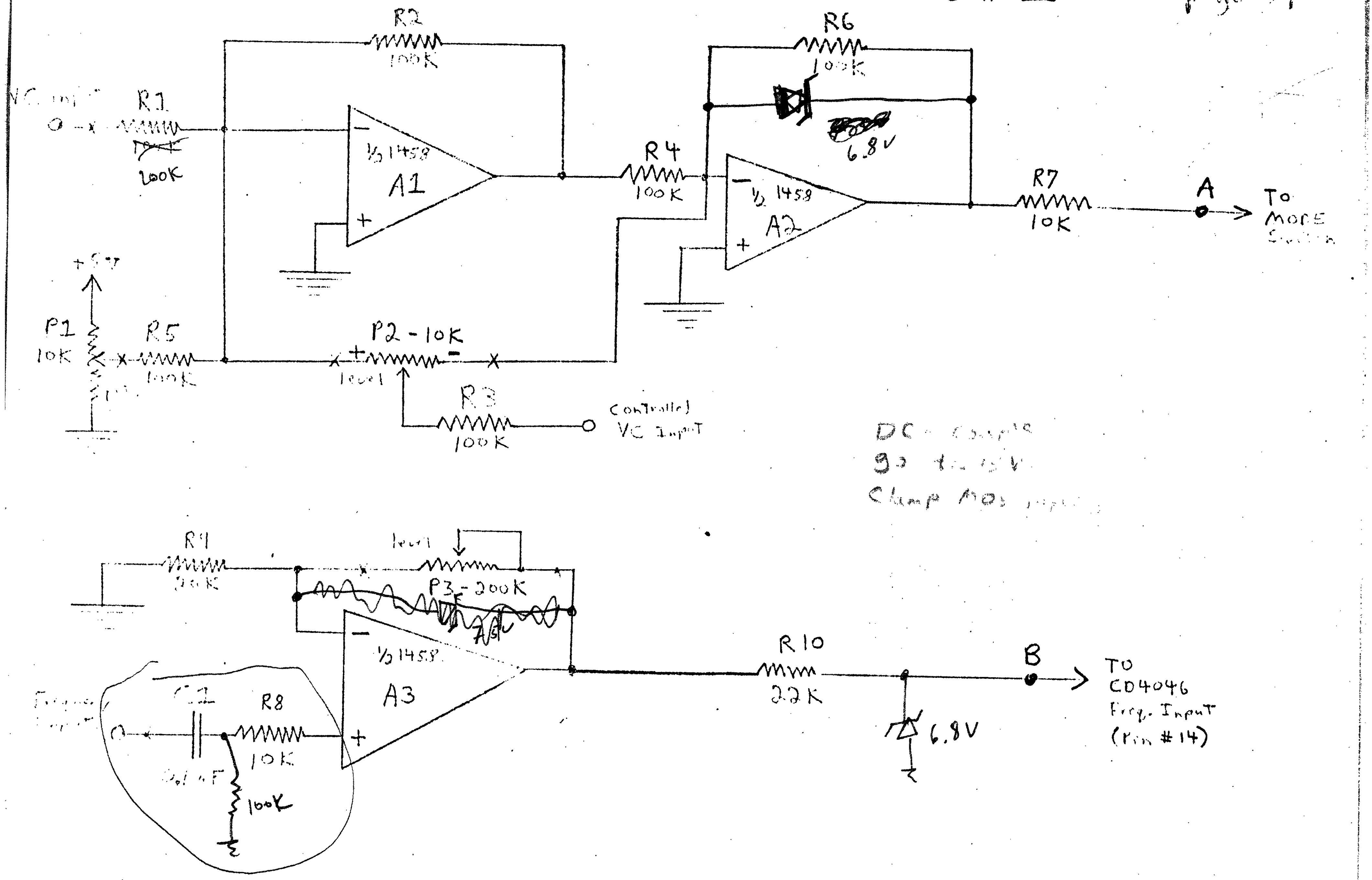
Controls:
- S1 Loop status (Open/closed)
- S2 Oscillator range (LFO/Audio)
- S3 Mode (VCO/PLL)
- S4 Capture time (multiple position switch)
- S5 Lock range (Low/High)
- P1 VCO frequency
- P2 VCO variable control input (+/-)
- P3 Frequency input gain
- P4 Oscillator output level
- P5 Loop Damping

LED's: LED1 PLL lock indicator

Uses: Used as a PLL, this module works as a "slave" tracking a master oscillator giving interesting "glide" and "bounce" effects. It can also be used as a linear VCO in both the audio and low LFO/clock ranges.

PHASE-LOCK LOOP

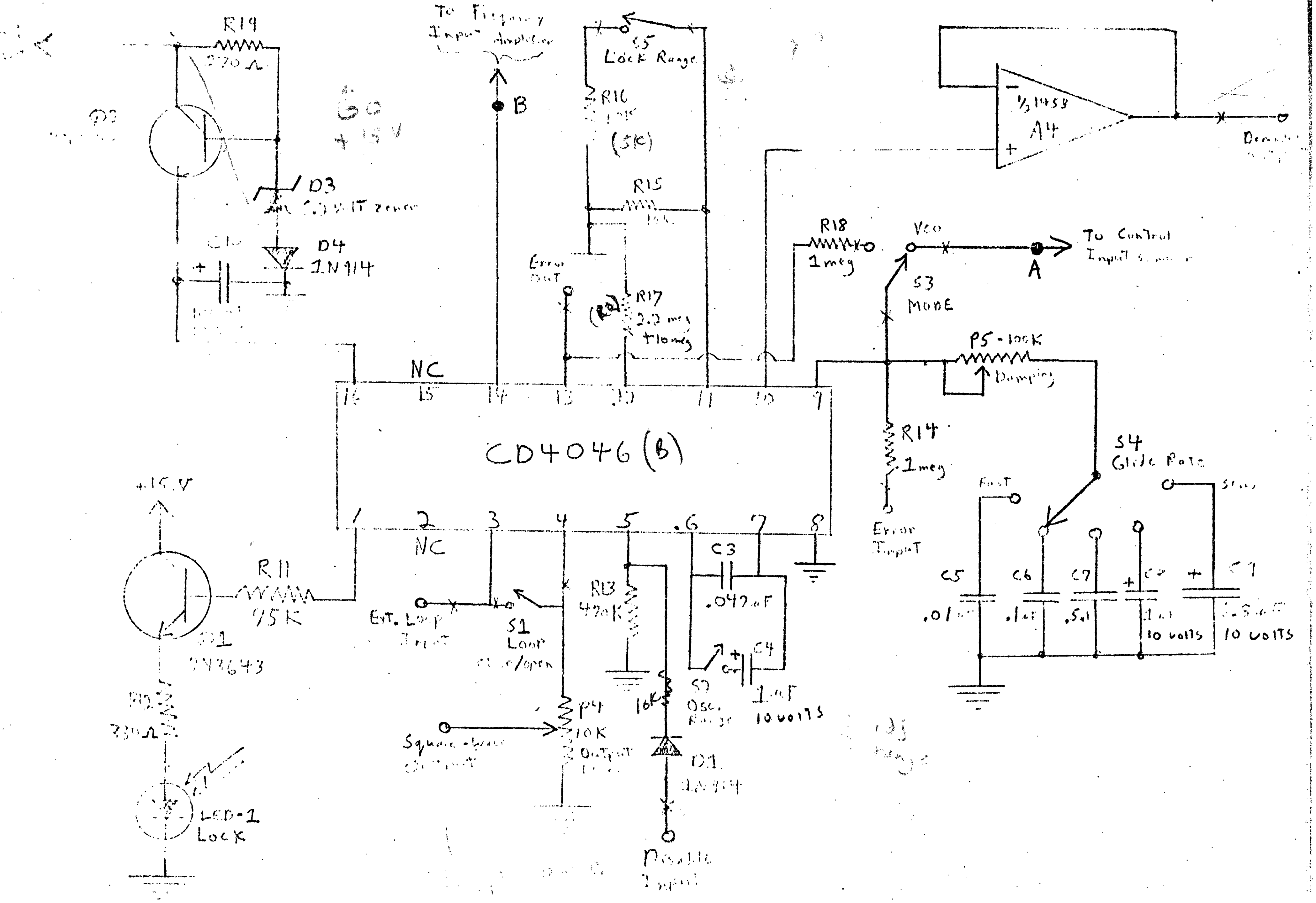
Schematic #1



Control Input Summer and Frequency Input Amplifier

PHASE-LOCK LOOP

Schematic #2



---Phase-Locked Loop/VCO---

When used as a PLL, A3 amplifies and buffers an input signal AC coupled through C1. The signal is input to the phase comparator of the CD4046 at pin#14. The loop filter runs between the phase comparator output (pin 13) and the VCO input (pin 9). The filter damping constant is set via P5, and its cutoff, thus "glide rate" is set via the capacitor selected on S4. An error signal may be input to the loop via R4.

R15 and R16 are timing resistors for the VCO, and its range may be altered via S5. Similarly C3 and C4 are VCO timing capacitors, and range can also be selected via S2.

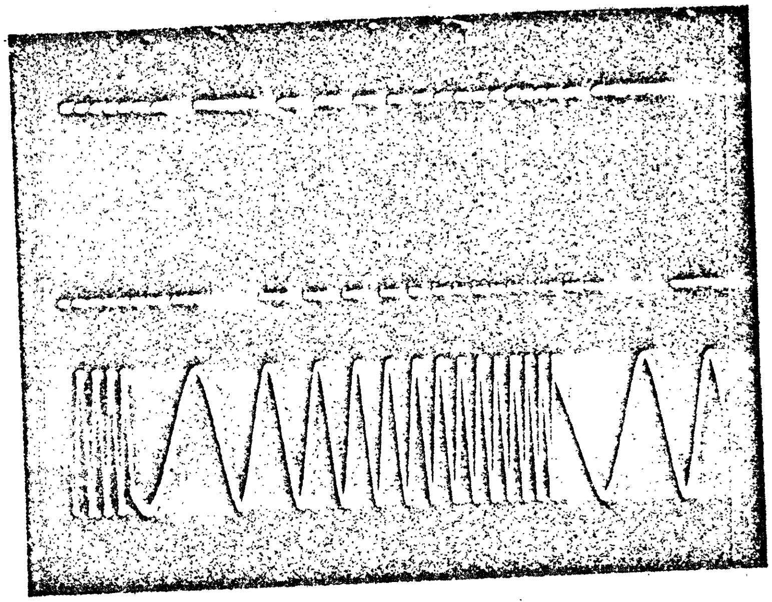
The phase comparator loop is closed through S1. If desired, S1 can be opened, and the feedback loop may be completed through external circuitry (binary divider, etc.). The rectangular wave output from pin#4 may be attenuated via P4. When the loop achieves lock, phase pulses are output at pin#1. These are buffered via emitter follower Q1 and fed to LED1, giving us a crude "lock" indicator. The high impedance demodulated output at pin 10 is buffered by voltage follower A4 before being exposed to the external world.

With S3 in the "VCO" position, the output of summing network A1/A2 is fed into the VCO input. "Rest" frequency is determined from the bias input at P1. R1 allows us a fixed control input, while P2 gives us a variable input with inversion capability.

The oscillator may be shut down by applying a voltage at the "disable" input through D1. A seven volt low impedance supply to drive the CD4046 is provided by series regulator Q2 and diodes D3 and D4, filtered through capacitor C10.

References:

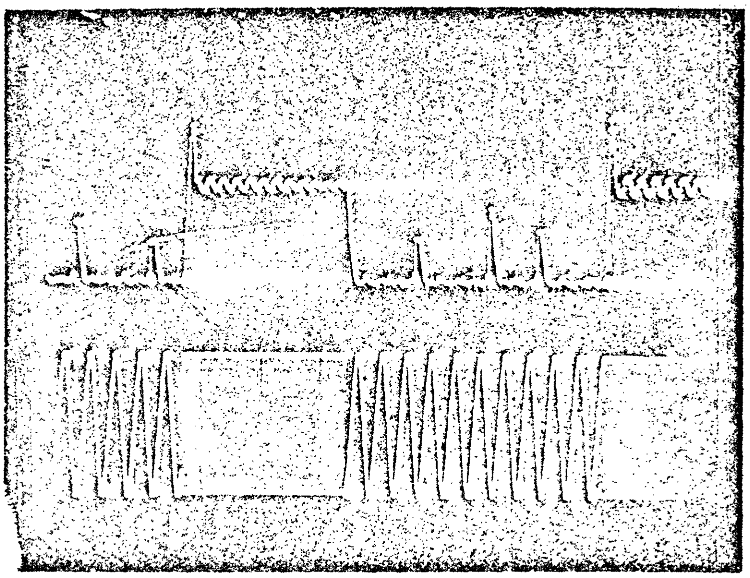
RCA COS/MOS Databook (1975)



PLL output

"Sweeping" sinusoid input to PLL

Photo#11 - PLL tracking an input frequency



Demodulated output from PLL (note ring oscillation)

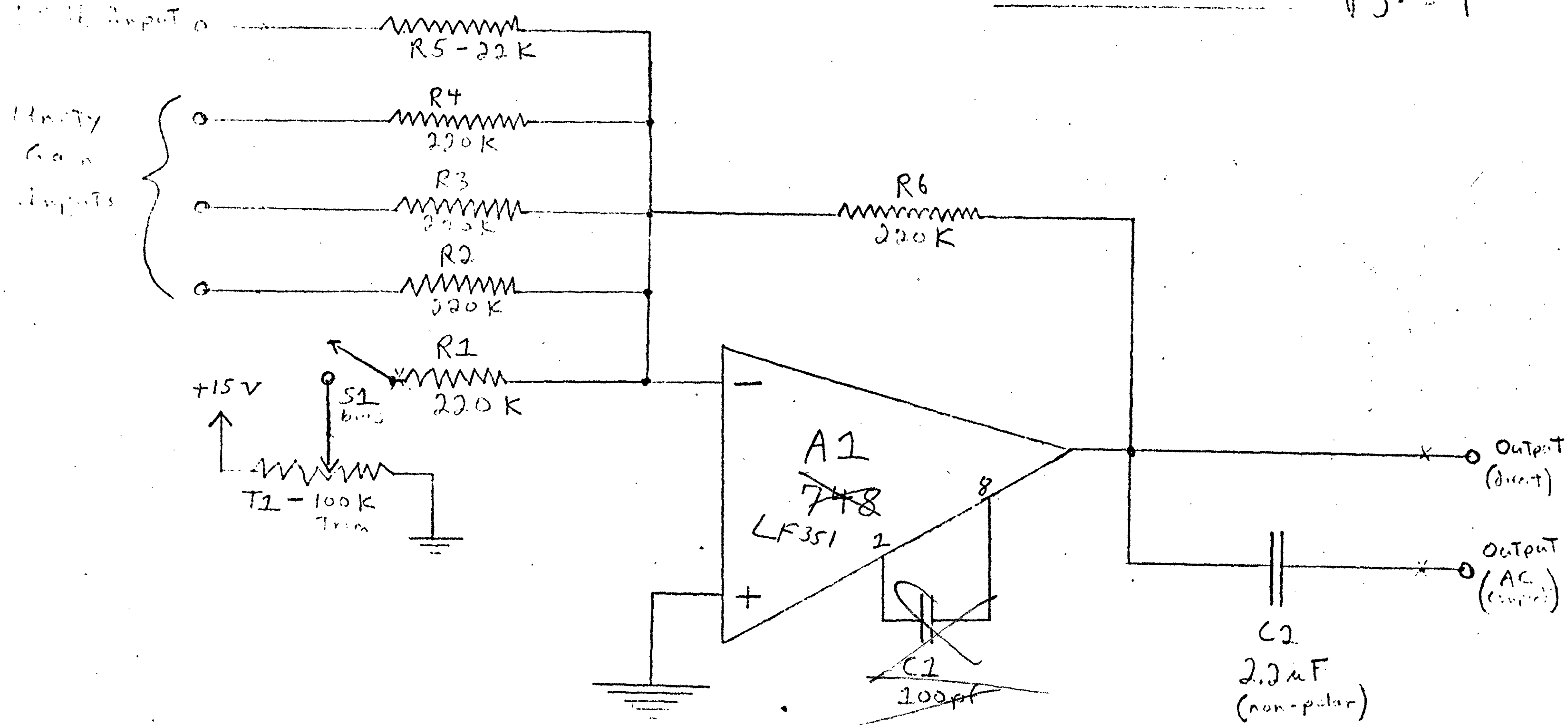
Waveform input to PLL

Photo#12 - The PLL as a frequency demodulator

5) INVERTING SUMMER

Inputs:	3 - 0 db unity gain 1 - 20 db (gain of 10)
Outputs:	Mix out (AC and DC coupled)
Controls:	S1 +5 volt offset (ON/OFF)
Uses	Simple mixer/inverter/amplifier. With offset switch, it can be used to invert logic signals.

INVERTING SUMMER



---Inverting summer---

This is a straightforward inverting summer. A1 sums inputs from R4, R3, and R2 at unity gain and weights an input through R5 with a gain of 10 (20 db). A bias may be pre-set on trimmer T1, and added to the mix via S1. C3 is provided for AC coupling.

References: NONE

6) ATTACK/DECAY TRANSIENT GENERATOR

Inputs: Trigger (initiate cycle)
Gate (hold high state)
Cycle re-set

Outputs: Transient output (direct, 0-8 volts)
Transient output (variable)
Inverted transient output (0-5 volts)
Attack gate (on during attack cycle only)
Attack end pulse (fires when attack concludes)
"Cycle over" gate (high when cycle finishes)

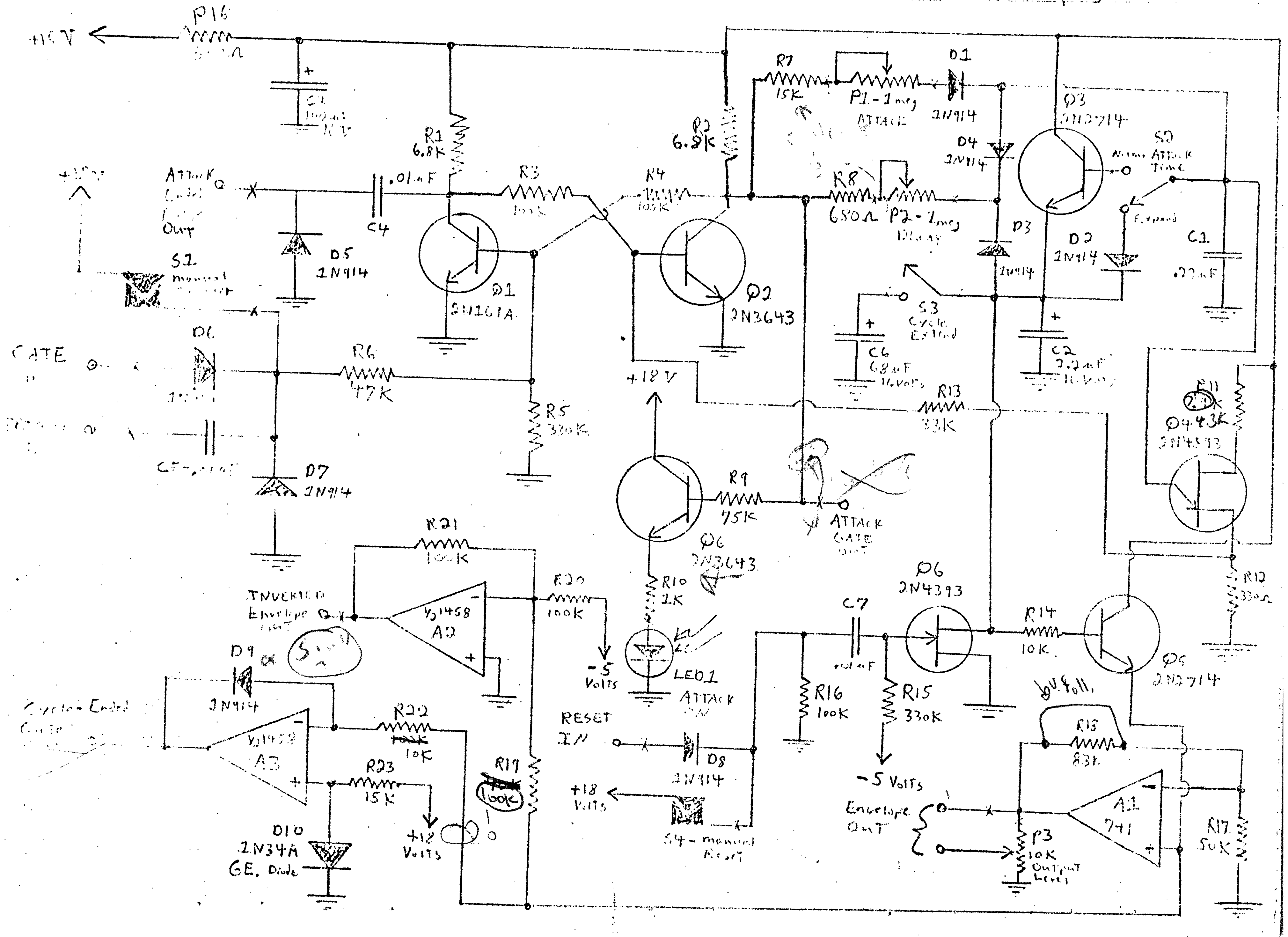
Controls:

S1	Manual trigger
S2	Attack rise (slow/fast)
S3	Cycle duration (0-10 secs./2secs-4min.)
S4	Manual re-set
P1	Attack time
P2	Decay time
P3	Variable output level

LED's LED1 Attack on

Uses: This module is very useful in creating a triggered envelope voltage. If the "cycle ended" gate is connected to the trigger input, it can be used as a relaxation oscillator.

ATTACK / DECAY ENVELOPE GENERATOR



--Attack/Decay envelope generator--

The heart of this circuit is the bistable multivibrator composed of Q1 and Q2. Normally Q1 is off and Q2 is on. When a pulse appears on the trigger or gate inputs however, the bistable changes state; Q1 turns on and Q2 turns off. Thus the voltage at the collector of Q2 goes high, and C1, C2, (and C6 if S3 is on) charges through P1, D1, and D2. (If the attack switch is in "normal" position, C2 will charge more quickly through current multiplier Q3, decreasing our attack time.) The collector voltage of Q2 is output as the "attack gate" and it is buffered through Q6 to drive LED1 as an indicator of the attack state.

The capacitors will charge until the voltage across C1 reaches the triggering threshold of UJT Q4. When this occurs, C1 discharges through Q4, producing a pulse across R12 which is fed back to the base of Q2. This turns Q2 on and places the bistable back into its original state. The collector of Q2 then goes low, and C2 (and C6 if S3 is on) discharges via D3 and P2. Thus the voltage across C2 exponentially attacks and decays with rates set by P1 and P2 respectively. This voltage is buffered by Q5 and amplified by non-inverting amplifier A1, appearing as our envelope output. It is also fed into inverter A2, where it is mixed with a DC offset via R20, appearing at A2's output as an "inverted" envelope. A3 is a comparator which compares the envelope waveform against the small (0.3 volt) potential across D10. Since D9 clamps the output positive, A3 generates a "cycle ended" gate which goes high upon the completion of an Attack/Decay cycle (when the envelope is less than 0.3 volts).

Q6 is an FET switch that shunts the transient capacitor, normally kept off via biasing resistor R15. The cycle may be re-set by inputing a pulse at the "re-set" input (or depressing S4), which is fed via C7 to the gate of Q6, turning it on briefly and discharging C2 (its internal resistance is too large to completely discharge C6).

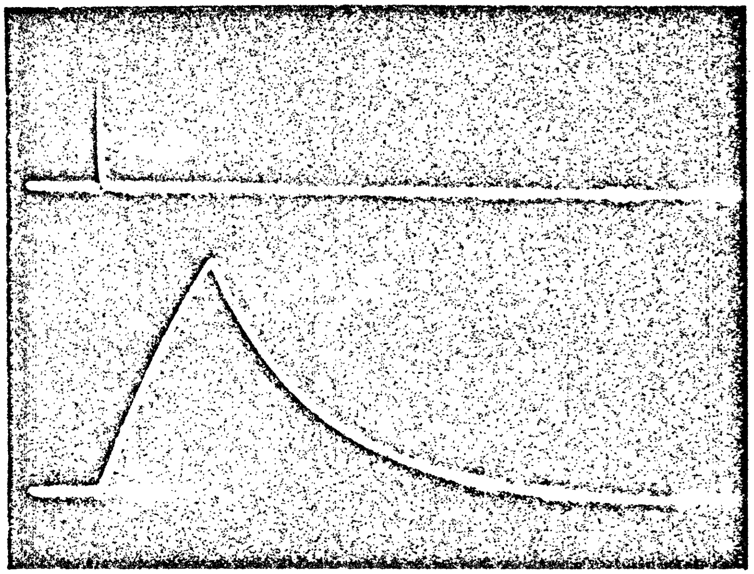
Additional notes... If the "gate input is held high, the bistable can not re-set, thus the envelope voltage saturates at its maximum level.

When the attack cycle ends, Q1 turns off. The collector voltage of Q1, therefore jumps high, and after it is differentiated by C4, we will recieve an "Attack ended" pulse output.

References:

Some basic design ideas appeared on page 102 of Radio-Electronics

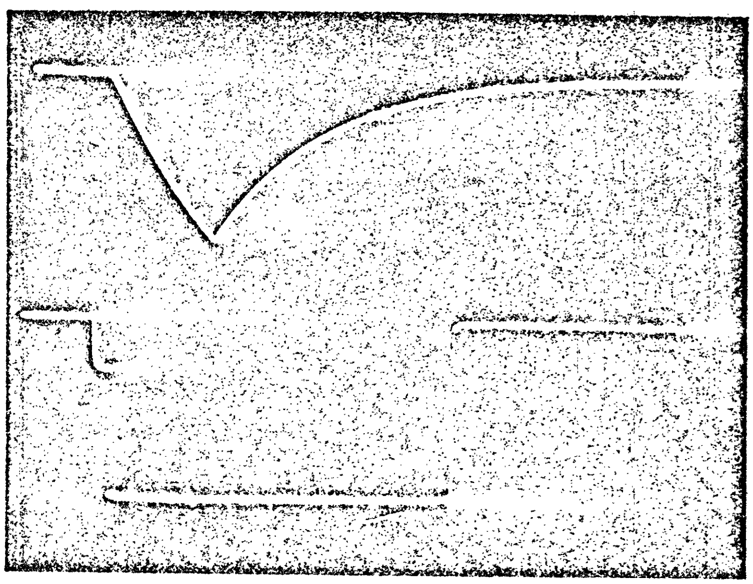
NOTE: Photo's 13, 14, and 15 were triggered by the same signal, and are in synch. They may be treated as timing diagrams.



Triggering pulse which initiates cycle

Normal attack/decay envelope output

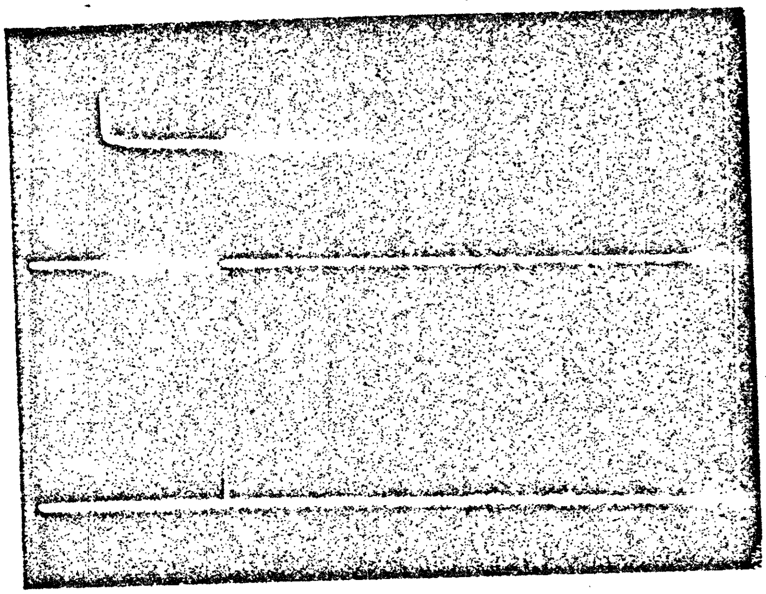
Photo#13 - AD module timing part 1



Inverted attack/decay envelope output

"Cycle ended" gate

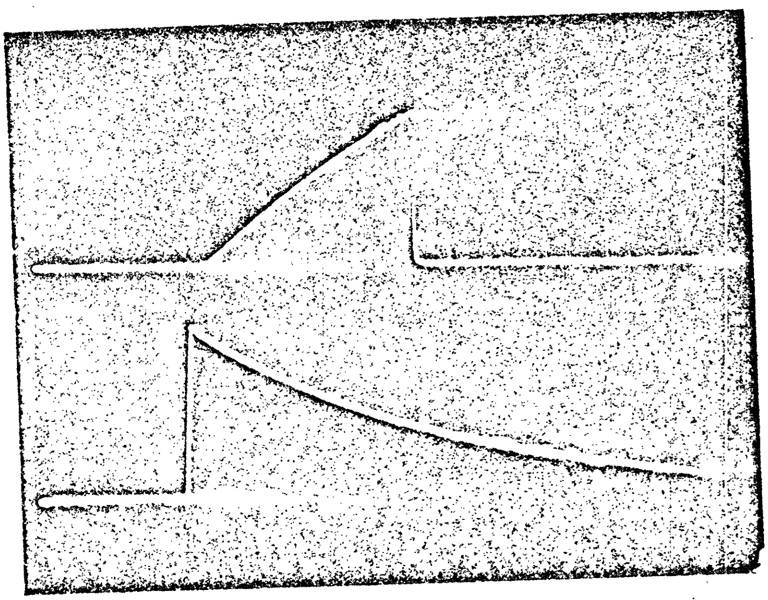
Photo#14 - AD module timing part 2



"Attack gate" output

"Attack ended" pulse output (the pulse is quite narrow, so it is very dim. It can be seen, however)

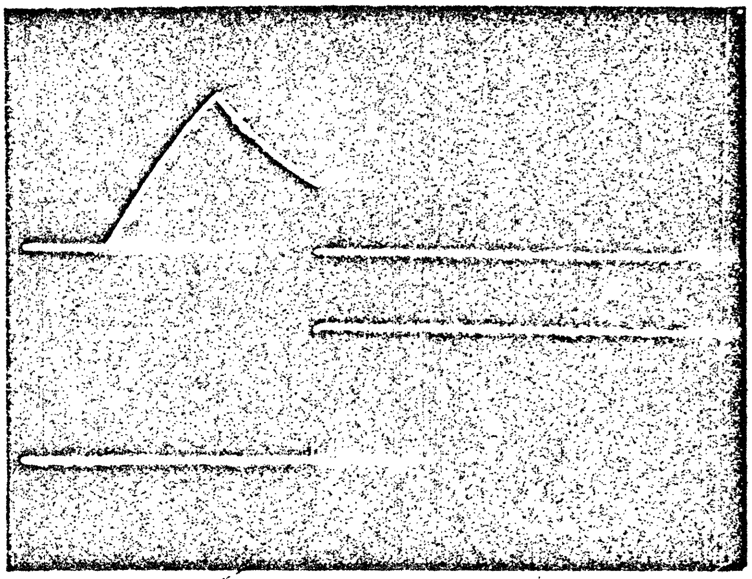
Photo#15 - AD module timing part 3



Slow attack, sharp decay

sharp attack, slow decay

Photo#16 - Envelope produced for different Attack/Decay settings



Output of envelope generator

"Step" applied to the re-set input

Photo#17 - Illustration of a step voltage re-setting the cycle

7) VOLTAGE CONTROLLED BANDPASS FILTER

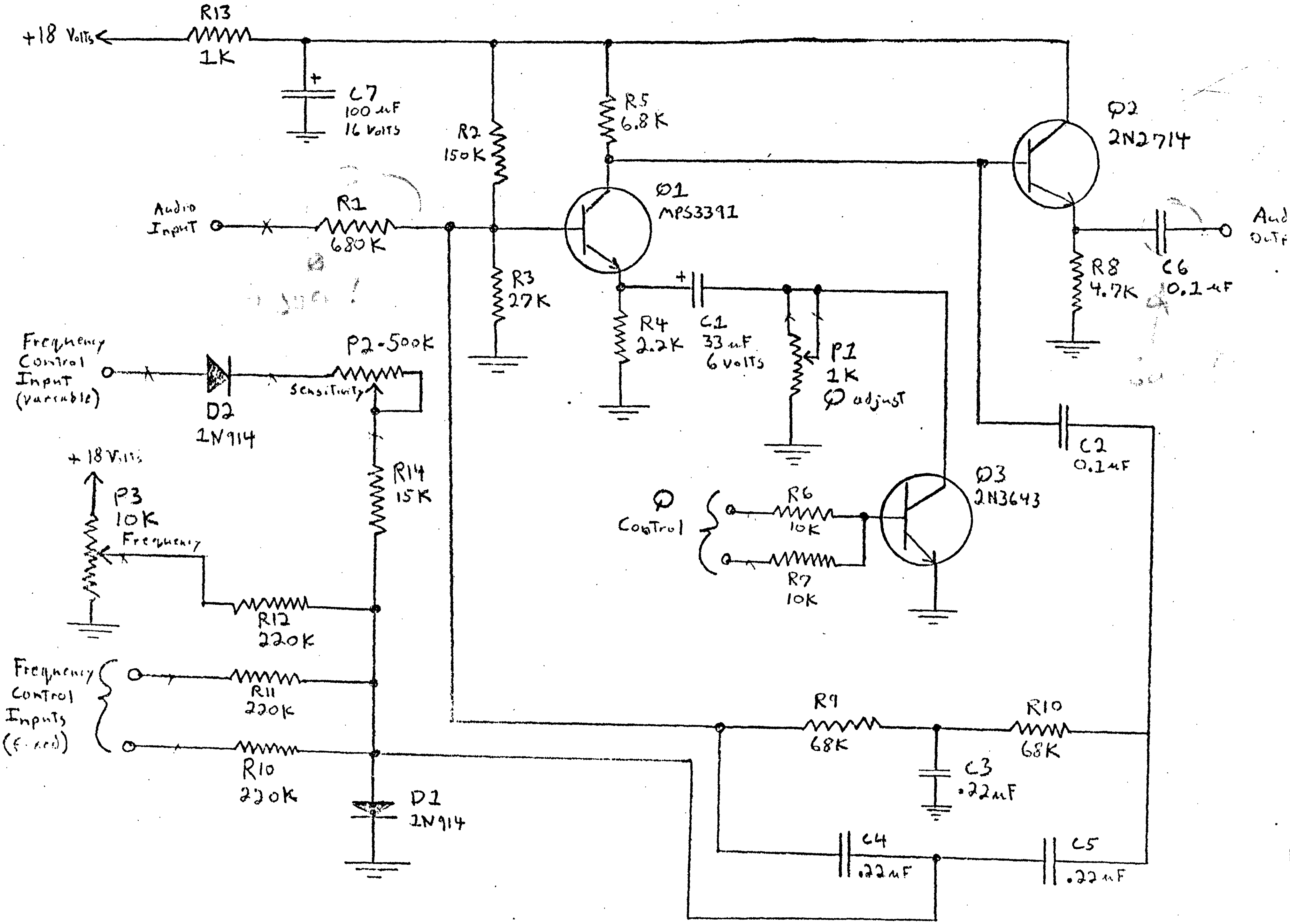
Inputs: Audio input
Fixed frequency control
Variable frequency control
Resonance (Q) control

Outputs: Audio output (filtered)

Controls: P1 Resonance (Q)
P2 Variable control sensitivity
P3 Center frequency

Uses: This filter has limited range and Q. It can be used as an auxilary filter, however, giving "wow"type sounds (typical of resonant filters), filtering noise to simulate percussion and wind, etc.

Band Pass Filter



---Voltage controlled bandpass filter---

The heart of this circuit is the paralell-T notch filter composed of R9, R10, C3, C4, C5, and the dynamic impedance of diode D1. The notch filter is connected in feedback across amplifier Q1. This gives us a bandpass response at the collector of Q1, which is buffered by emitter follower Q2 and is coupled to the output via C6.

Control inputs are summed with the frequency bias set by P3, causing DC current to flow through D1, thus setting D1's operating point on its characteristic and determining its dynamic impedance. The impedance of D1 determines the center frequency of our filter.

The resonance depends upon the gain of Q1. This can be adjusted by varying the AC emitter bypass via P1. Q3 also shunts the emitter, and a voltage at the "Q control" inputs will turn it on, thus increasing our resonance.

R13 and C7 provide de-coupling from the "noisy" 18 volt supply.

References:

The original circuit was proposed in the September 1973 issue of Radio-Electronics

8) VOLTAGE CONTROLLED LOWPASS FILTER

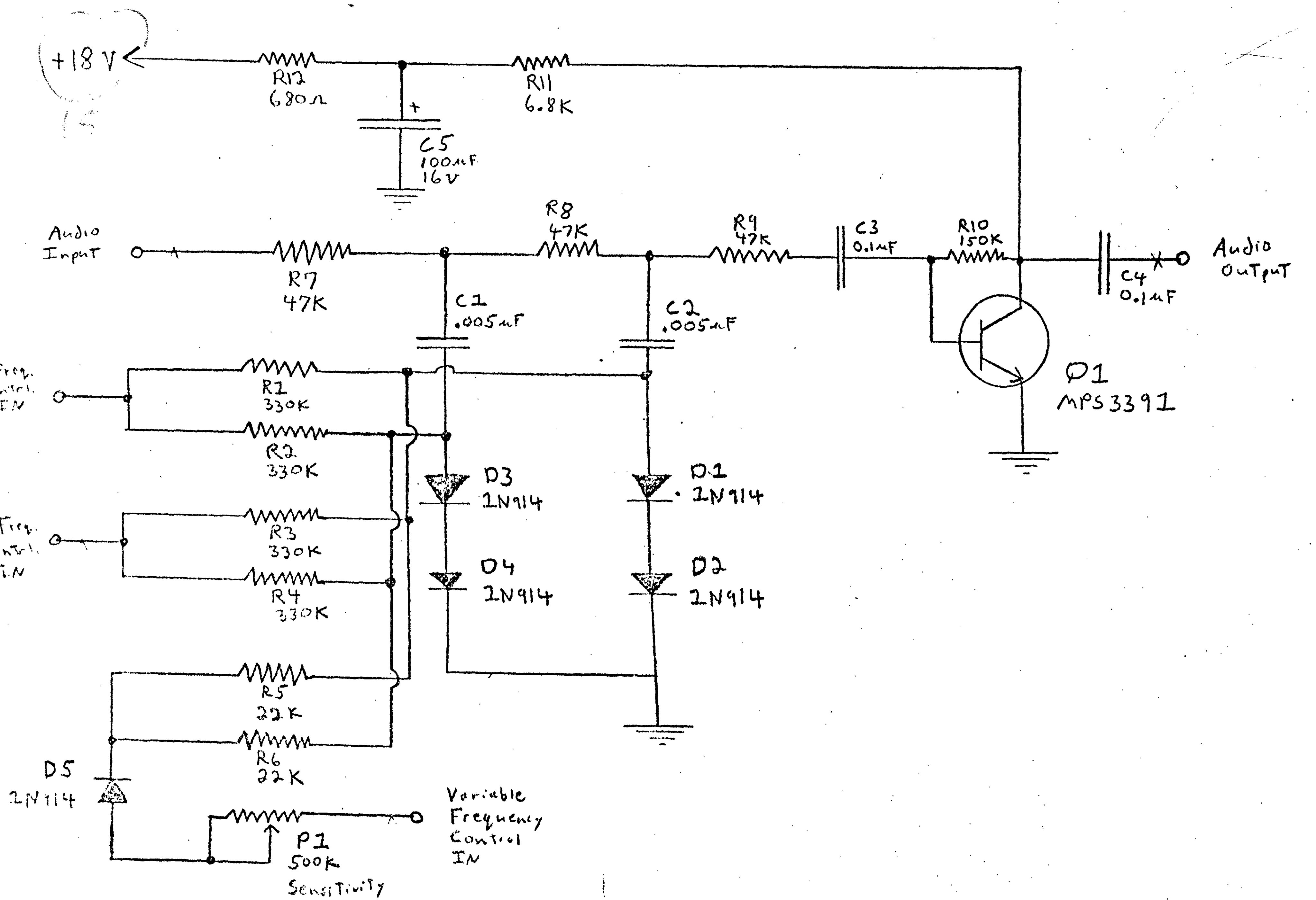
Inputs: Audio input
Fixed frequency control
Variable frequency control

Outputs: Audio output

Controls: P1 Variable control sensitivity

Uses: This filter is a simple Lowpass with no resonance. It can be used to selectively remove higher harmonics from a frequency rich signal.

LOW PASS FILTER



---Voltage controlled lowpass filter---

An audio signal is input to the double-ganged (in order to increase roll-off) passive low-pass filter networks (R7/C1 and R8/C2). The conductance through the capacitors, thus the cutoff froquency of the filter, is determined by the dynamic impedance of diodes D1-D4. This impedance is set by the DC current flowing through D1-D4, which is due to the voltages on the control inputs. Q1 is a simple grounded-emitter amplifier which makes up for the losses encountered in the passive filter network. The audio output is AC coupled through C4.

References:

The original circuit was proposed in the September 1973 issue of Radio-Electronics

9) BANDPASS VCF WITH LFO

Inputs;	Audio input Frequency control Resonance (Q) control LFO frequency control
Outputs:	Audio output (filtered) LFO output (sinusoid)
Controls:	Filter center frequency Resonance (Q) Filter frequency control input sensitivity LFO frequency
Uses:	Filter has very limited range and Q, useful for "wows" etc. LFO sine output is very handy as a control voltage.

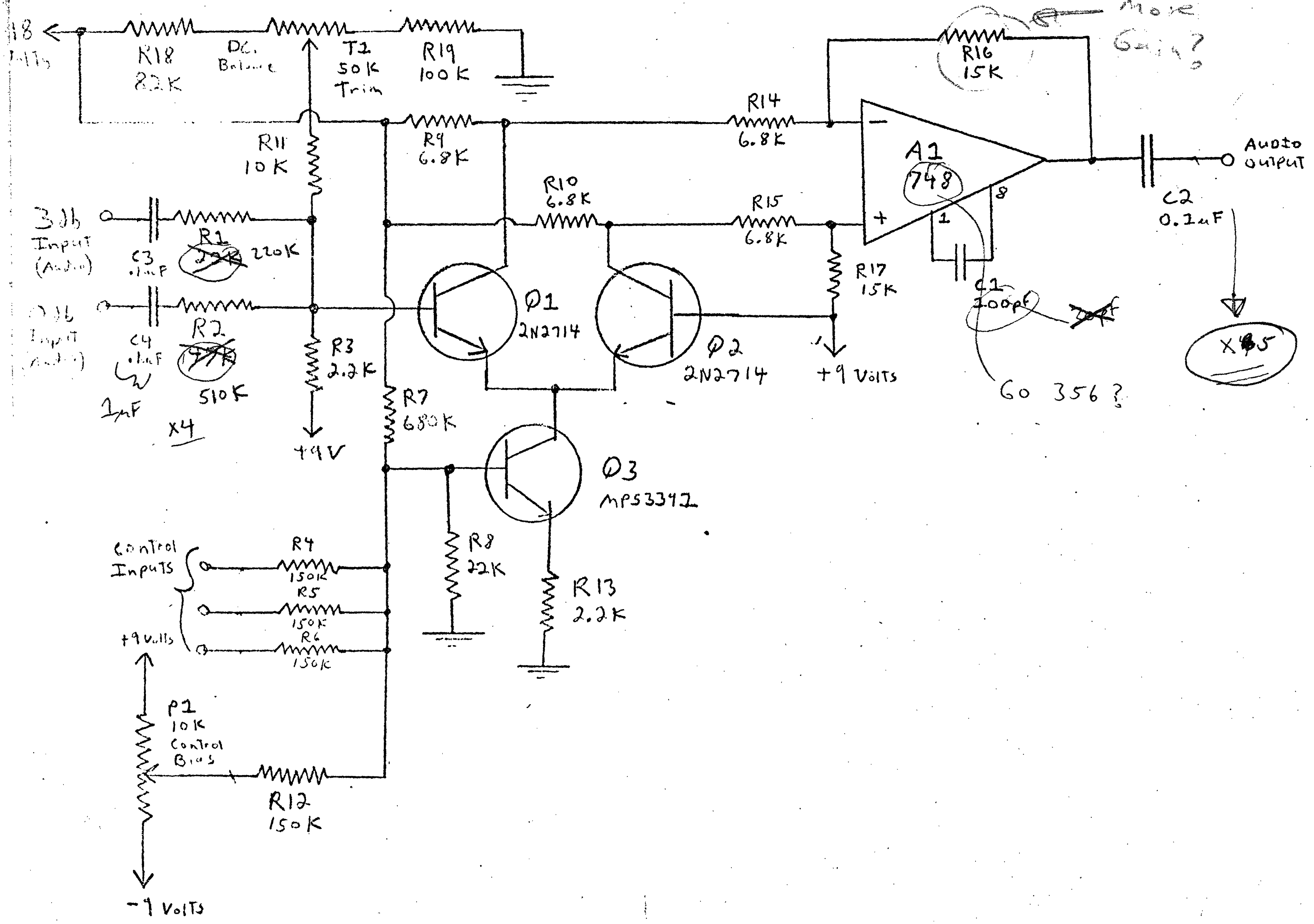
---Bandpass VCF with LFO---

This circuit was based upon a diagram appearing in a 1969 issue of Popular Electronics as a "Leslie Effect Simulator". I have long since lost all diagrams and documentation on the circuit, and, since it is not often used, I won't attempt to re-construct a schematic. The essence of the device is a bandpass filter, with a frequency-controlling resistance determined by the dynamic impedance of a FET. The circuit also outputs a low-frequency voltage-controlled sinusoid, which can prove valuable for control applications.

10) AC COUPLED VCA

Inputs:	Unity gain signal input (AC) 3 db gain signal input (AC) Amplitude control
Outputs:	Signal output
Controls:	P1 Control-bias
Uses:	This module is one of the handiest on the synthesizer. It is used to dynamically control the amplitude envelope of an audio signal (usually in conjunction with a transient generator). It is actually an AC coupled two quadrant multiplier.

Voltage Controlled Amplifier

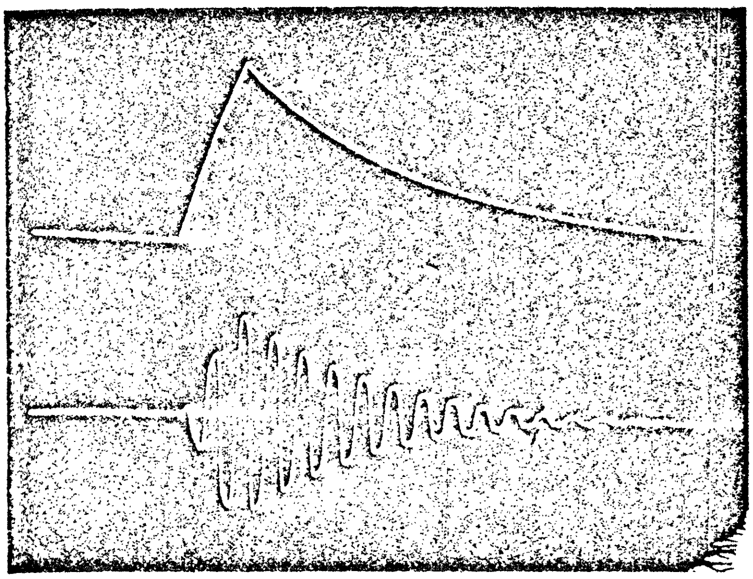


---AC coupled VCA---

In this circuit, an audio signal is input to differential pair Q1/Q2 via resistors R1 and R2 (R2 is selected for unity gain, R1 will give 3db). The gain of the pair is determined by the collector bias currents flowing through R9 and R10. This current flows through the collector of Q3, and its magnitude is set by the current flowing into Q3's base. Thus the voltages at the control inputs and the control bias from P1 control this current and the gain of the circuit. Differential amplifier A1 converts the voltage difference across Q1 and Q2 into an output with respect to ground. Because of the transistor biasing, all inputs and outputs are AC coupled. Trimmer T1 is adjusted to null the DC offset in the audio line due to mismatch between Q1 and Q2.

References:

Original circuit proposed in September 1973 issue of Radio-Electronics.



Control voltage input to VCA

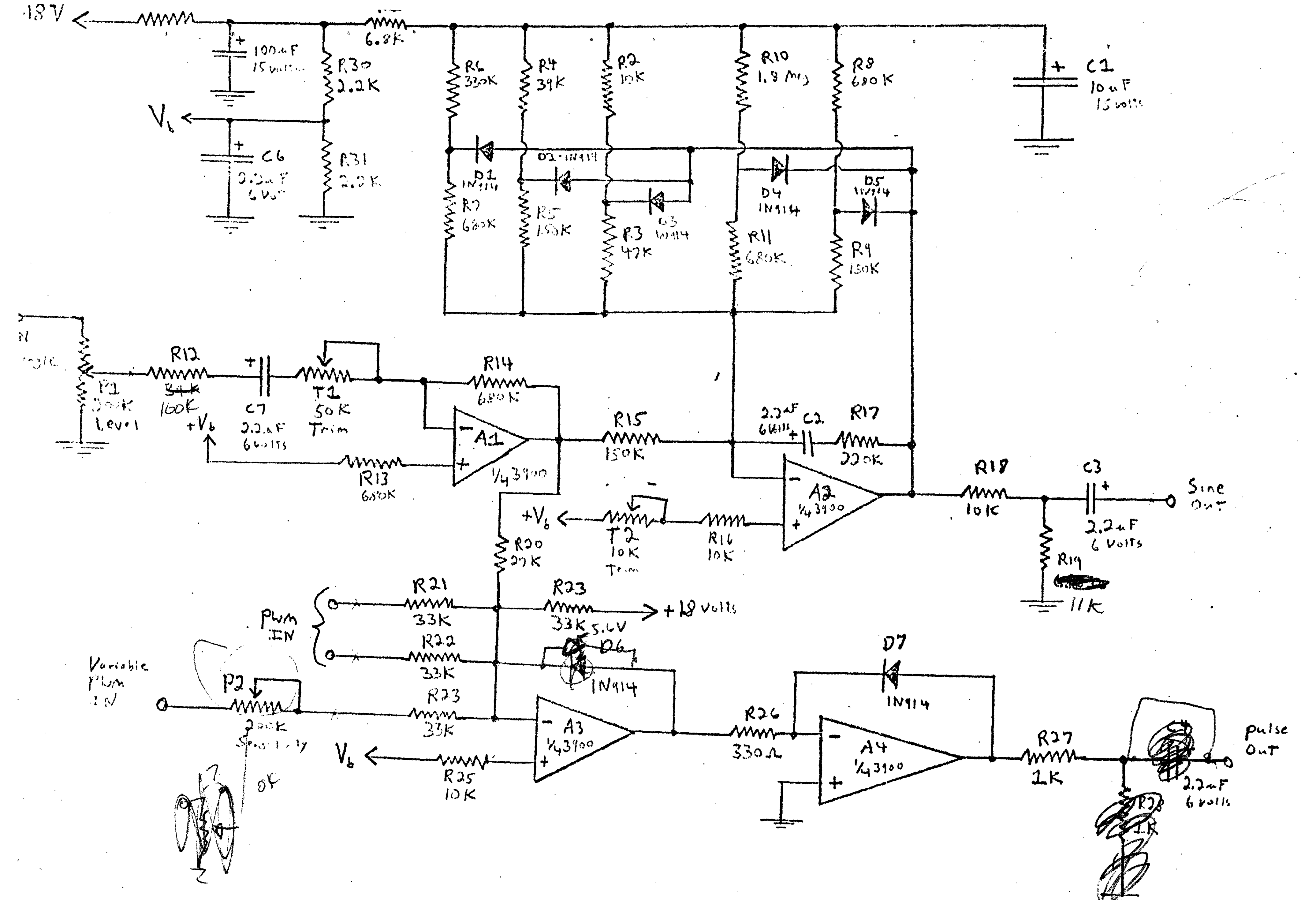
Output of VCA

Photo#18 - VCA - (A sine wave is applied to the audio input)

11) PULSE WIDTH MODULATOR/SINE SHAPER

Inputs:	Signal input (usually triangle wave)	
	Pulse width control (fixed)	
	Pulse width control (variable)	
Outputs:	Rectangular pulse	
	Shaped sinewave	
Controls:	P1	Signal input level
	P2	Variable pulse width control sensitivity

Uses: Dynamically alters harmonic spectrum via duty cycle control. Diode shaping circuit can yield sine wave with triangle input, or clipped waves with other inputs.



Triangle → Sine Shaper / Pulse Width Modulator page 60

----Pulse width modulator/Sine shaper----

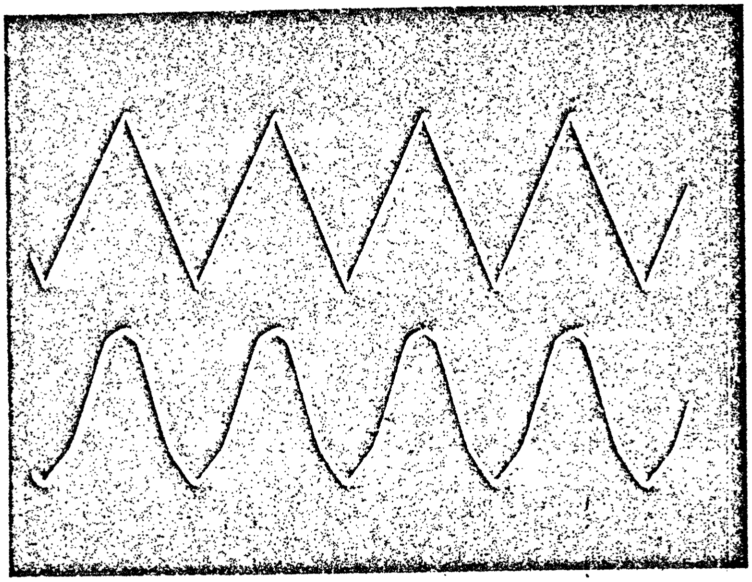
This circuit employs a Current Differentiating Norton Amplifer, the LM3900. A1 is a buffer which amplifies an input (triangle wave), with gain set by T1 and P1. This buffered triangle wave is then summed with "PWM" input currents flowing through R21-R23 and P2 at the '-' input of A3. A3 is a comparator which switches high when the current into the '+' terminal (set by a constant bias source) surpasses the current into the '-' terminal (set by our triangle wave and control voltages). The control voltages, then, determine the point on the triangle wave at which the comparator switches, modulating the pulse width at the comparator's output. Diodes D6 and D7 clamp the pulse to 1 volt peak and provide bias current in the '-' amplifier inputs.

The triangle wave is also fed to A2, which is a conventional inverting amplifier with a diode-shaping network in its feedback loop. R3-R11 are voltage dividers which set the break-points on diodes D1-D5. As each diode conducts, the gain of A2 changes, effectively "shaping" our sinusoid. The DC offset added to the triangle in A2 is determined by the bias current flowing through T2 and R16. T2 is adjusted so that the break-points will occur at the proper positions on the waveform, thus determining the "purity" of our sinusoid.

R30 and R31 form a voltage divider to produce the biasing voltage used in the CDA's. Since CDA's are designed to run from a uni-polar supply, all inputs and outputs are AC coupled to protect biasing.

References:

Original circuit proposed in a 1973 issue of Radio-Electronics



Triangle wave input to shaping network

Shaped "sinusoid"

Photo#19 - Sine shaper in action

12) ENVELOPE FOLLOWER

Inputs: Audio input (low level)

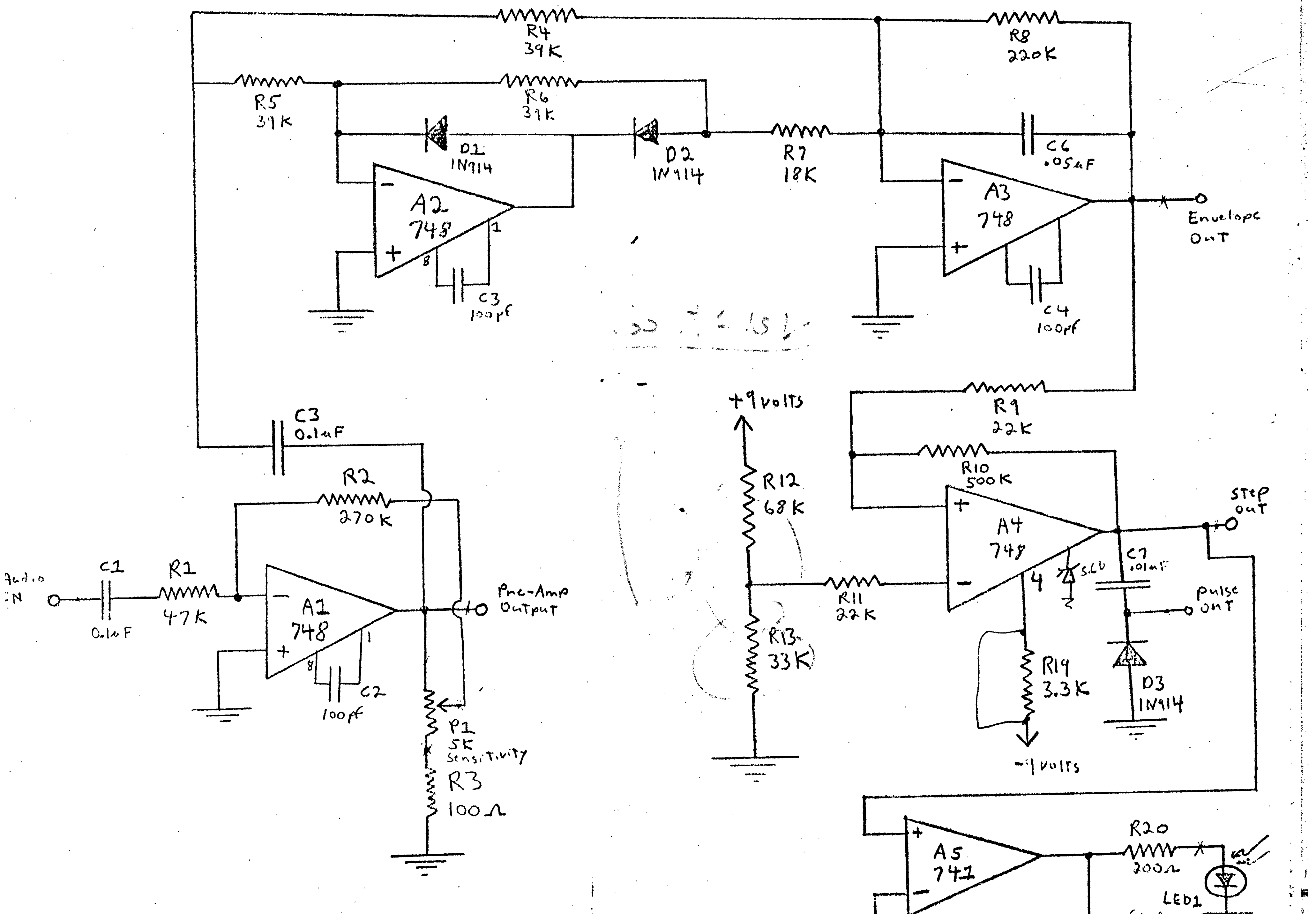
Outputs: DC envelope of input signal
Envelope comparator gate
Envelope comparator pulse
Amplified input signal

Controls: P1 Audio input gain

LED's LED1 Envelope comparator triggered

Uses: An external audio source (ie. microphone, etc.) may be input via this module, which pre-amplifies the signal while outputing a DC voltage proportional to its amplitude. A comparator switches high when this envelope exceeds a pre-set value.

ENVELOPE FOLLOWER



---Envelope follower---

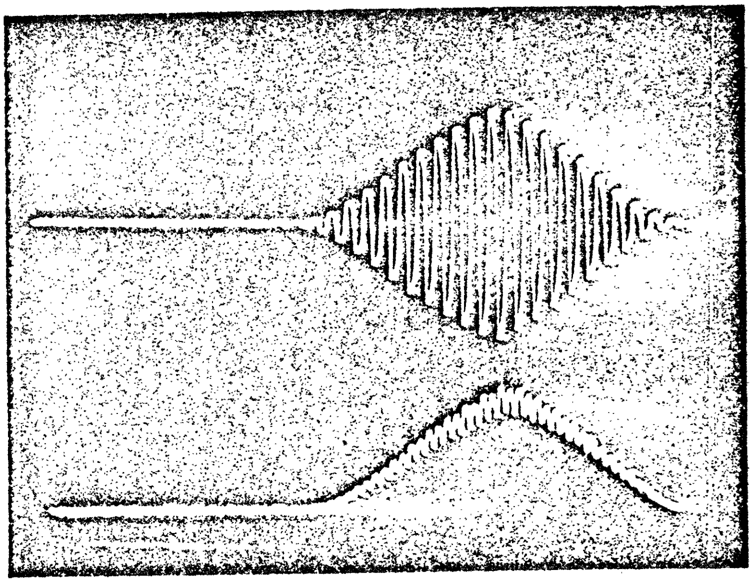
A low-level audio input is amplified by A1, with gain set by P1. The output of A1 appears as the "pre-amplified output" and is fed into clamper A2. The sum of the original input via R4 and the clamped output of A2 via R7 yields a full-wave rectified signal at the input of lowpass filter A4. This lowpass filter "detects" the amplitude envelope of the input signal, and its output appears at the "envelope out" terminal. R12 and R13 are a voltage divider which provide a reference voltage to comparator A4. When the envelope exceeds this reference, the output of A4 goes high, giving us our "step output". This is differentiated by C7, forming our "pulse output". The step is also buffered by voltage follower A5 which drives LED1, giving us an optical indication of comparator triggering.

R10 gives A4 a margin of hysteresis, which prevents stray triggering on noise in the envelope. The V- supply of A4 is fed through R19, which limits its negative output swing.

References:

Original circuit proposed by PAIA Electronics

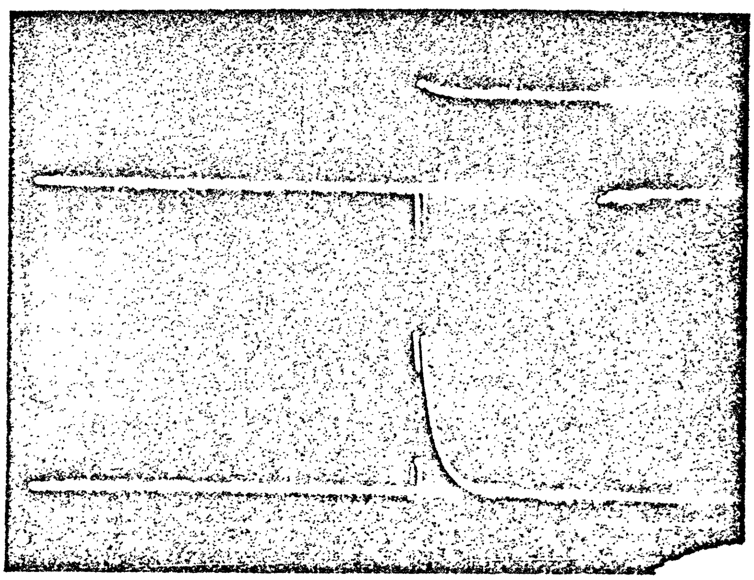
NOTE: Photographs 20 and 21 were triggered in synch, and may be considered as timing diagrams.



Waveform input to envelope follower

Amplitude envelope output

Photo#20 - Envelope follower timing part 1



Comparator gate out

Comparator pulse out

Photo#21 - Envelope follower timing part 2

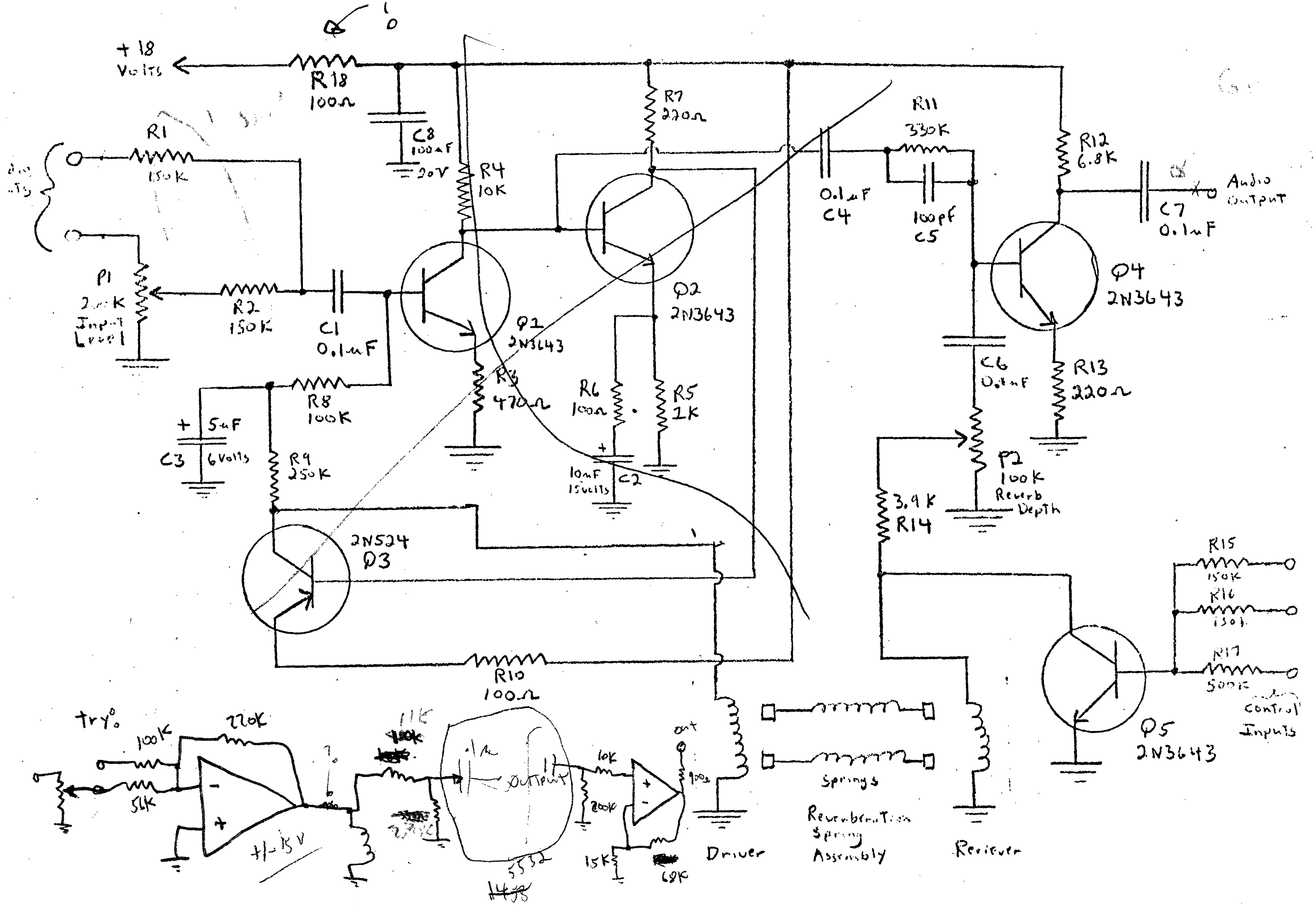
13) REVERBERATION AMPLIFIER

Inputs: Audio input (fixed)
Audio input (variable)
Reverberation "depth" control

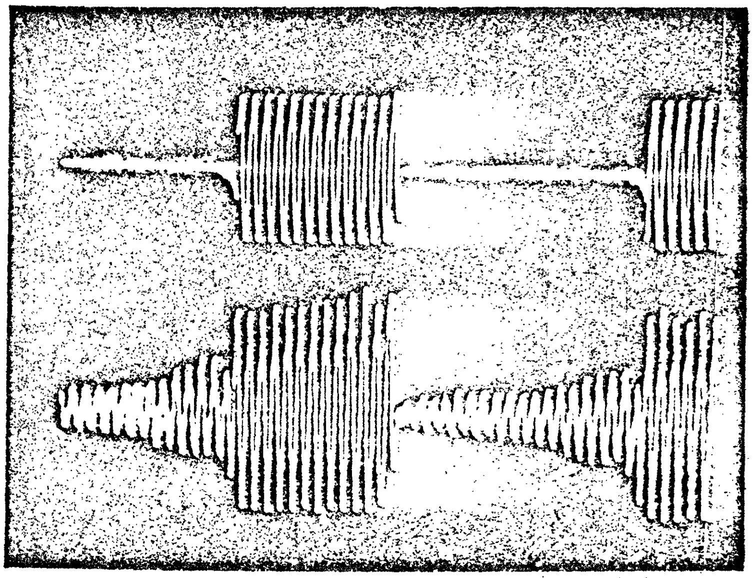
Outputs: Reverberated signal output

Controls: P2 Reverberation depth
P1 Variable audio input attenuator

Uses: Spring reverberation tray adds "concert hall" depth to sound. Amount of reverberation may be voltage controlled.



Reverberation Amplifier (with voltage-controlled reverb)



Tone "bursts" input to the reverberator

Output of reverberator (reverberation is obvious)

Photo#22 - Reverberated signal

upside down!

14) DISTORTER

Inputs: Audio input
Distortion control input

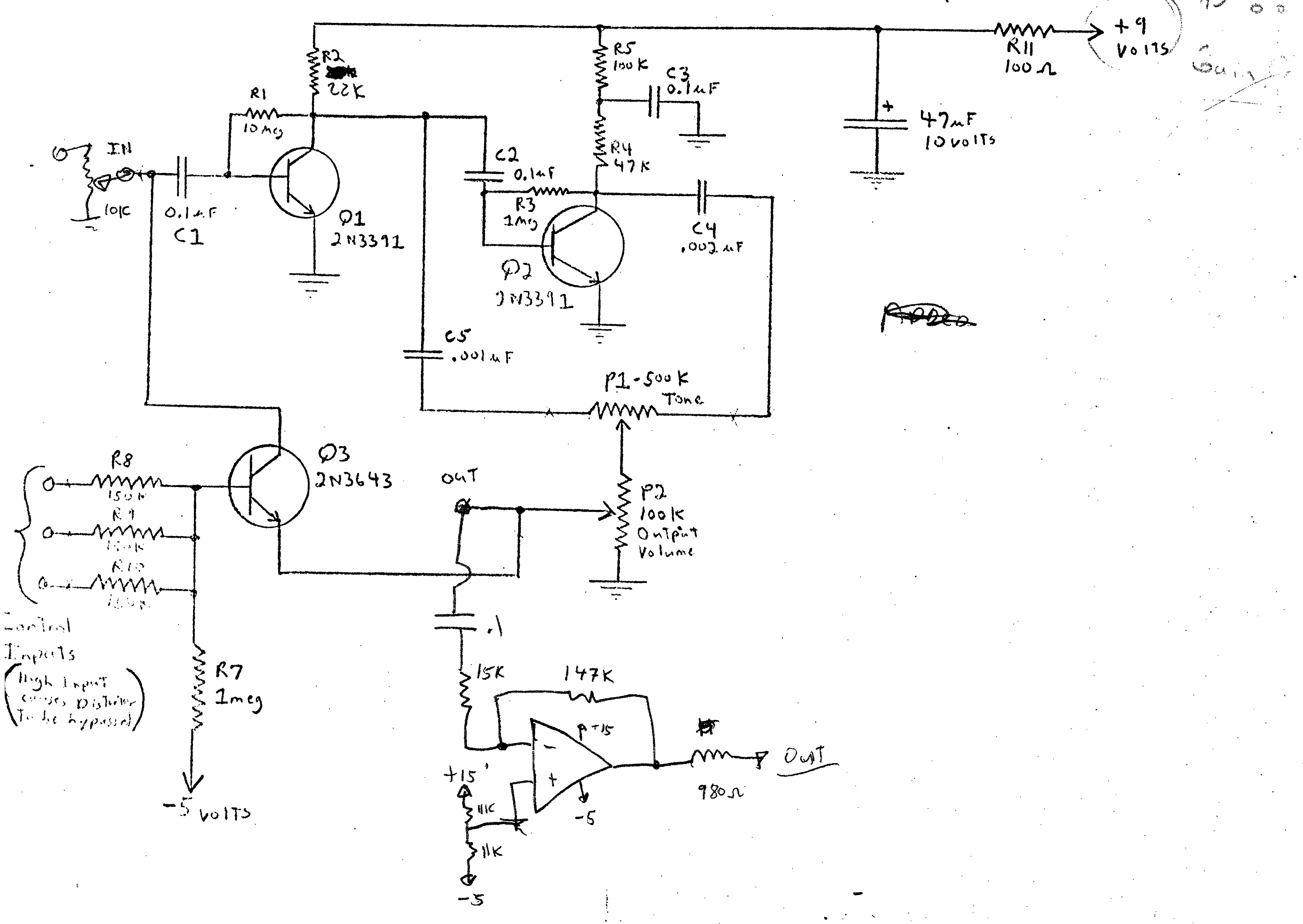
Outputs: Distorted signal out

Controls: P1 Distortion "tone" control
P2 Output level

Uses: This module modifies an input signal to provide a unique "distorted" sound. The Input/output signal mix may be voltage controlled, providing dynamic control over the distortion level.

DISTORTER

page 92

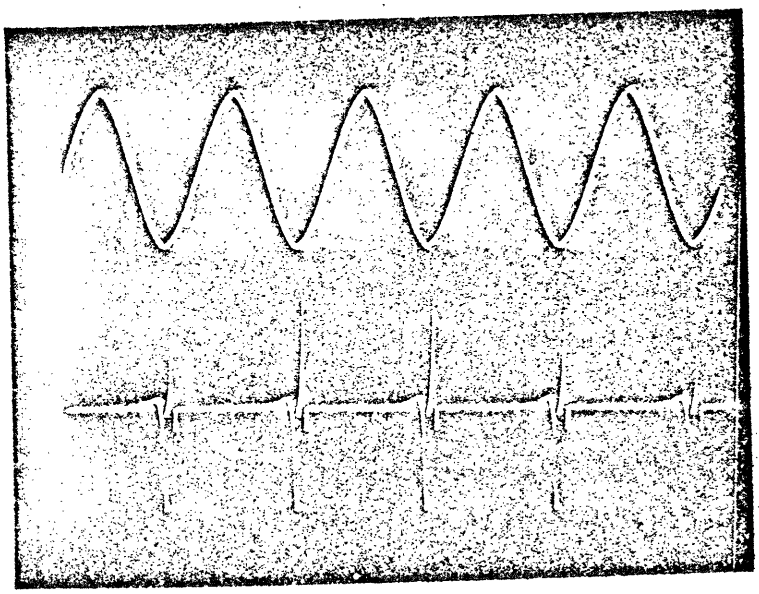


---Distorter---

The input signal is differentiated via C1 and fed to the base of high-gain comparator Q1. Q1 switches on whenever the slope of the input changes from positive to negative, producing a long, narrow "spike". This spike is fed to the base of another high-gain amplifier Q2, which compliments it, and, because of C3, filters it. The collector outputs of both Q1 and Q2 are summed in "tone" control P1. P2 attenuates the output. Q3 shunts the entire circuit, and when a positive signal is applied to its base via the control inputs, the input waveform passes through the collector "undistorted" to the output terminal.

References:

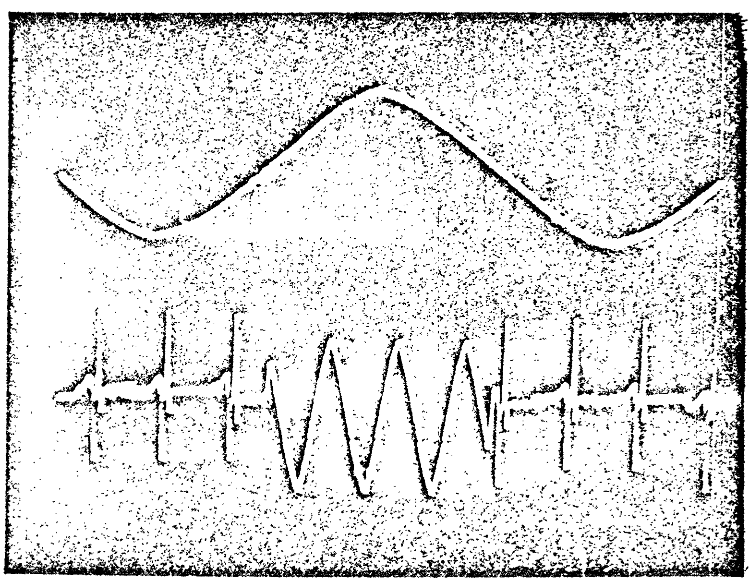
Circuit based upon a design by Wurlitzer Co.



Sine wave input to distorter

Distorter output

Photo#23 - Distorted sine wave



Control voltage input to distorter's control input

Distorter's output

Photo#24 - Voltage controlled distortion
(A sine wave is input to the distorter's audio input)

15) SAMPLE/HOLD

Inputs: "Sampled" signal input
Sample trigger input
Sample gate (for track/hold operation)

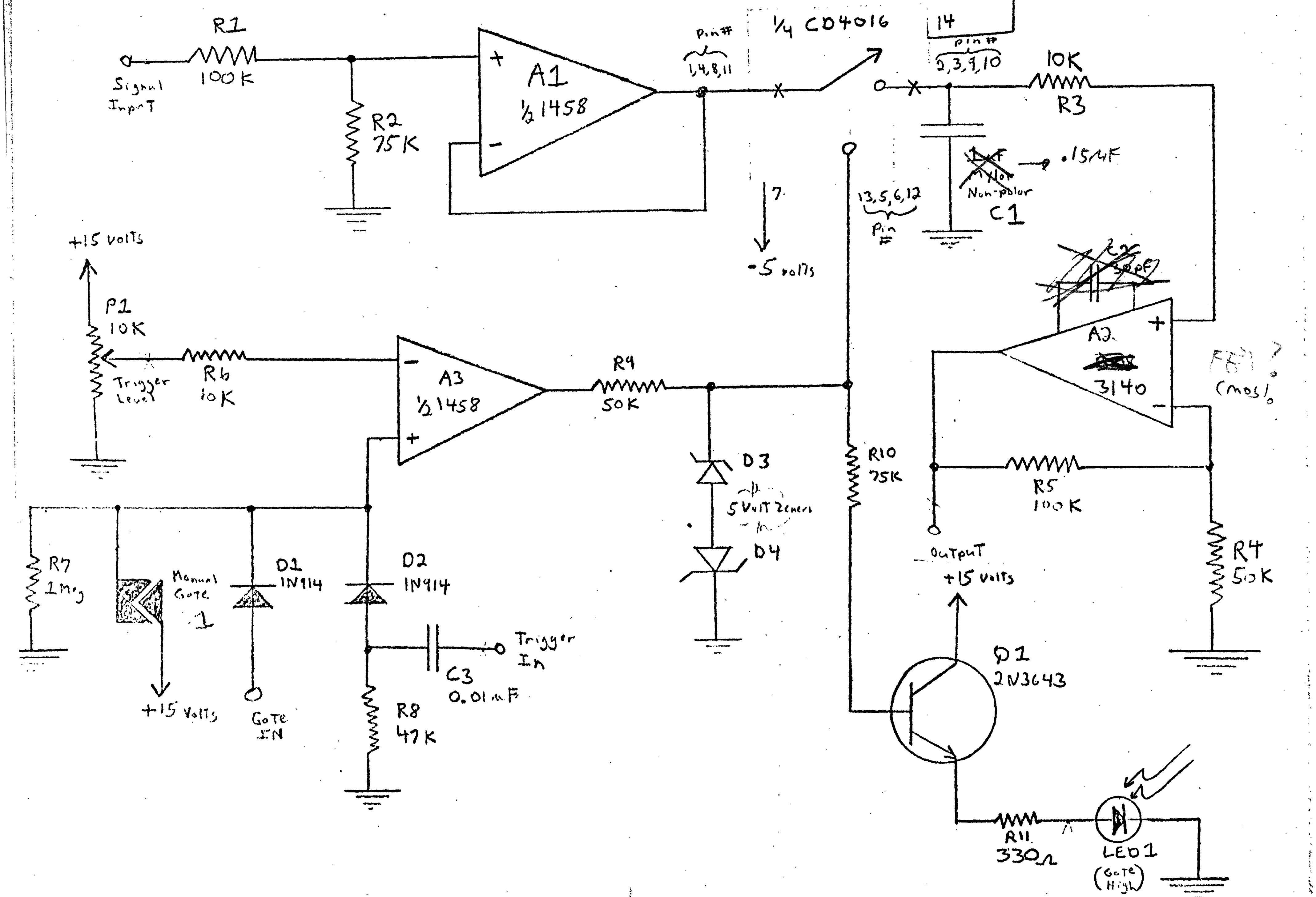
Outputs: Sample/hold out

Controls: P1 Sample trigger threshold
S1 Manual sample trigger

LED's LED1 Sample trigger high

Uses: If a periodic signal is input, it can be clocked and made to produce sequentially repeating control voltages. With the noise generator, random voltage steps can be obtain

Sample - Hold



R1
100K
Signal Input
R2
75K
A1
½ 1458
Pin #
1,4,8,11
¼ CD4016
14
Pin #
2,3,9,10
+5 volts
10K
R3
.15μF
Non-polar
C1
7
-5 volts
13,5,6,12
Pin #
+15 volts
P1
10K
Trigger Level
R6
10K
A3
½ 1458
R4
50K
D3
5 Volt Zeners
D4
R10
75K
A2
3140
FET?
(mos)
R5
100K
R4
50K
Output
+15 volts
Q1
2N3643
R7
1 Meg
Manual Gate
+15 Volts
D1
1N914
Gate IN
D2
1N914
C3
0.01μF
Trigger In
R8
47K
R11
330Ω
LED1
(Gate High)

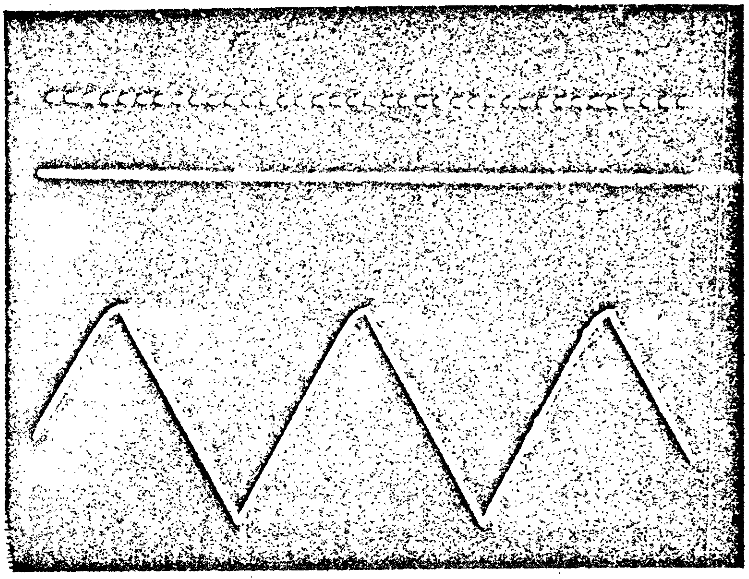
---Sample/Hold---

NOTE: This is a dual module containing two of these circuits. (They both share the same CD4016 package, however.)

The input signal is attenuated via divider R1/R2 to bring it into the -5 to +5 volt range. It is then buffered by voltage follower A1 and fed to the CMOS analog switch. When this switch is closed, we are in "track" mode, and the voltage across hold capacitor C1 follows the input. Non-inverting amplifier A2 buffers C1, and provides gain to boost the voltage back to its original level (before the R1/R2 divider). When the analog switch is off, the only leakage paths open for C1 are through the switch or via the '+' terminal of A2. The leakage through the CMOS switch is negligable, and A2 is an LM308, posissing ultra-low input bias currents. Thus the voltage on C1 is held constant, and the output of A2 is kept at the last sampled point.

A3 is a comparator which drives the trigger circuitry. When the trip voltage at the '+' input surpasses this level, the comparator goes high and closes the CMOS switch. Voltage is applied to this poin via D1 (gate), S1, or C3 and D2 (differentiated pulse trigger). D3 and D4 clamp the control to +/- 5 volts, the limit for the CMOS switch (since it is run from a bipolar 5 volt supply). This voltage is buffered by Q1 and input to an LED which is activated whenever we enter "sample" or "hold" mode.

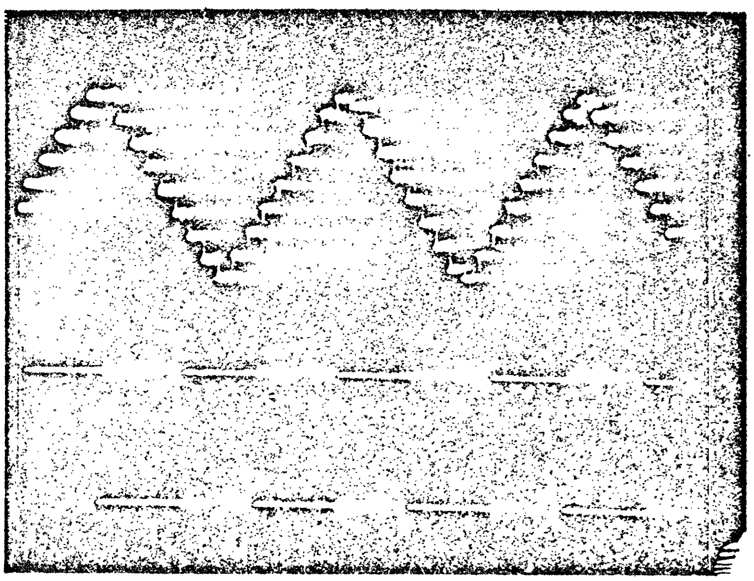
References: NONE



Pulse input to trigger on S/H

Triangle wave at the sampled input of S/H

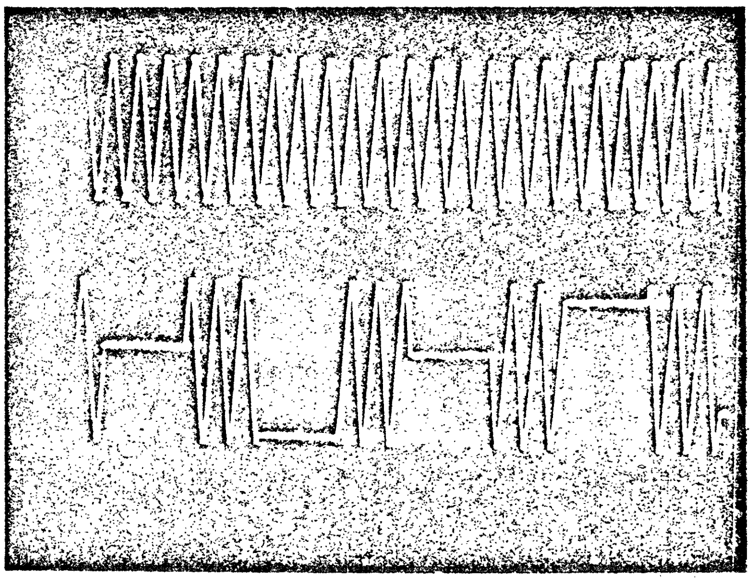
Photo#25 - Waveforms input to S/H to yeild output shown in Photo#26 part A



Part A:
Output of S/H when waveforms in photo#25 are input

Part B:
Square wave applied to the gate input of S/H to yield photo#27

Photo#26 - Sample hold



Waveform at S/H's sample input

Output of S/H with above wave at input and the square wave in Part B of Photo#26 at the gate input

Photo#27 - Track and hold operation

16) NOISE GENERATOR

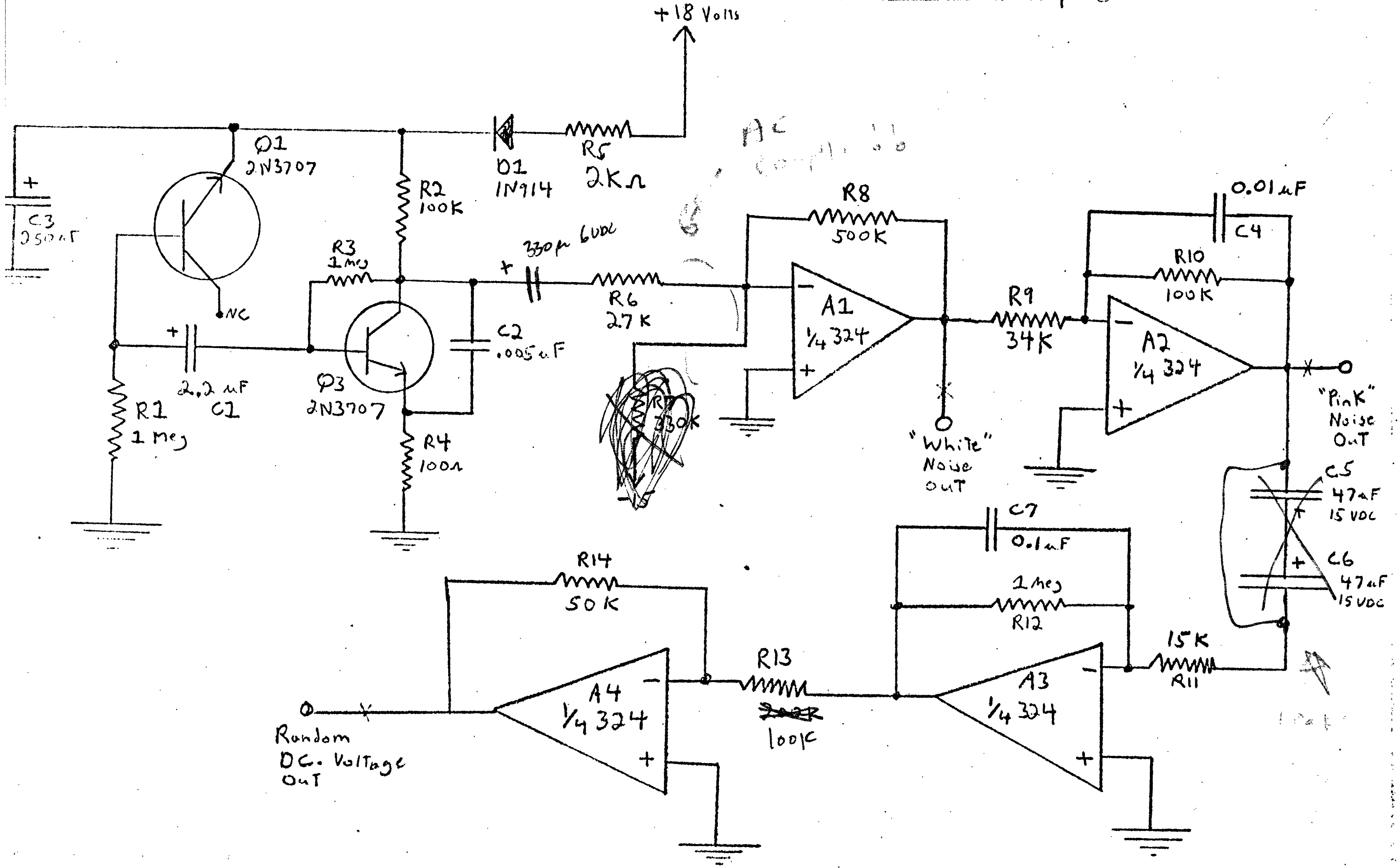
Inputs: NONE

Outputs: White noise
Pink noise (White noise filtered through LP. filter with 1 khz rolloff @ 20 db/decade)
Random DC (Pink noise filtered through LP filter with 10 hz rolloff @ 20 db/decade)

Controls: NONE

Uses: Noise produced by EB breakdown of NPN silicon transistor. White noise can be used for percussion and wind effect, etc. Pink noise can be used for percussion, wind, surf, explosion and so on. Random DC can be used wherever a randomly varying control voltage is needed.

NOISE SOURCE



---Noise Generator---

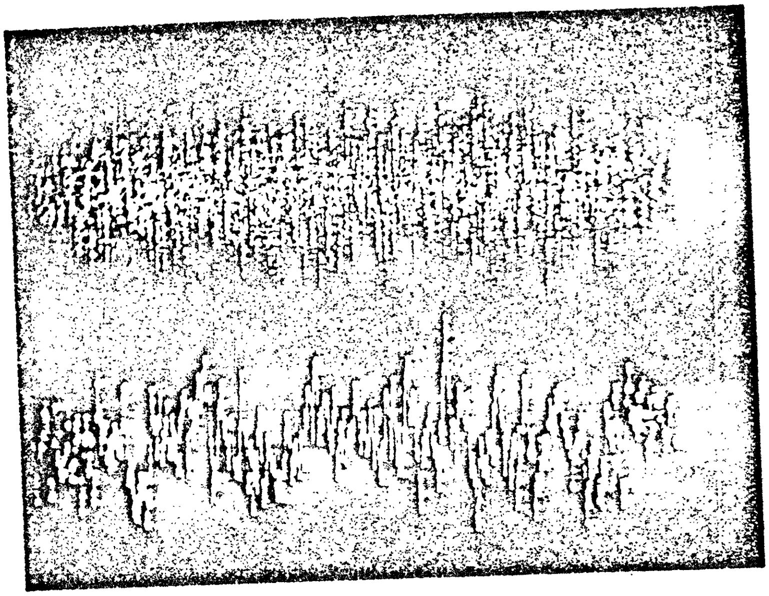
NOTE:This is a dual module containing two of these circuits.

Since the emitter of a bipolar transistor is heavily doped, reverse-bias avalanche breakdown of the emitter-base junction generally occurs at 15 to 20 volts. Here we are using the +18 volt supply to breaddk down Q1. Avalanching is quite noisy in transistors, and the noise in Q1's reverse current is detected by R1 and boosted by amplifiers Q3 and A1 (R7 supplies a bias to normalize the noise to ground.) . The output of A1 appears as 5 volt p-p "white" noise. This white noise is passed through low-pass filter A2, which rolls off 20 db/decade at 1 khz. The output of A2 is bassier "pink noise". The DC and ultra low frequencies presént in this signal are blocked by C5 and C6, and then fed into low-pass filter A3, which rolls off at 10 hz. This signal is buffered and attenuated to useable limits by A4 and appears as a slowly varying "random DC" voltage.

Because of the high gains involved, this circuit is particularly sensitive to power supply noise. D1, R5, and C3 do a good job of de-coupling.

References:

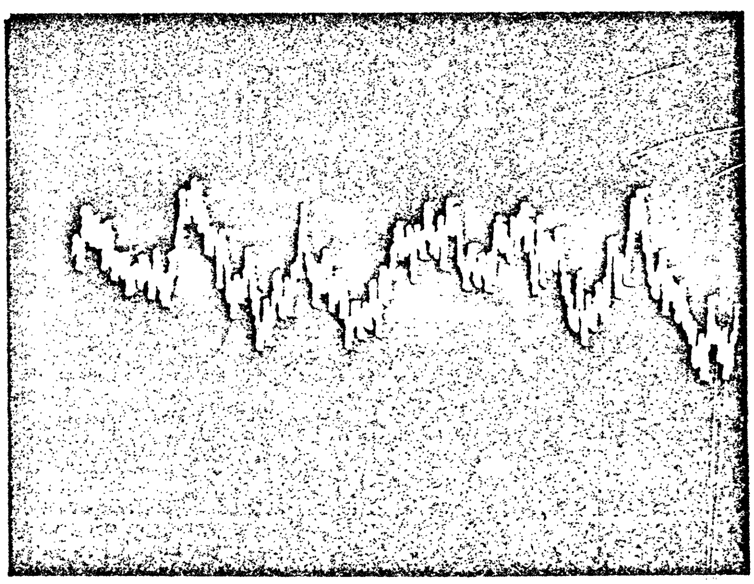
The basic Q1/Q2 noise generator is based on a design proposed by PAIA electronics.



"White" noise

"Pink" noise

Photo#28 - Noise generator outputs



"Random DC voltage"
(The sweep time on this photograph is much slower than the rate used in photo#28

Photo#29 - Noise generator outputs

17) PHASE SHIFTER

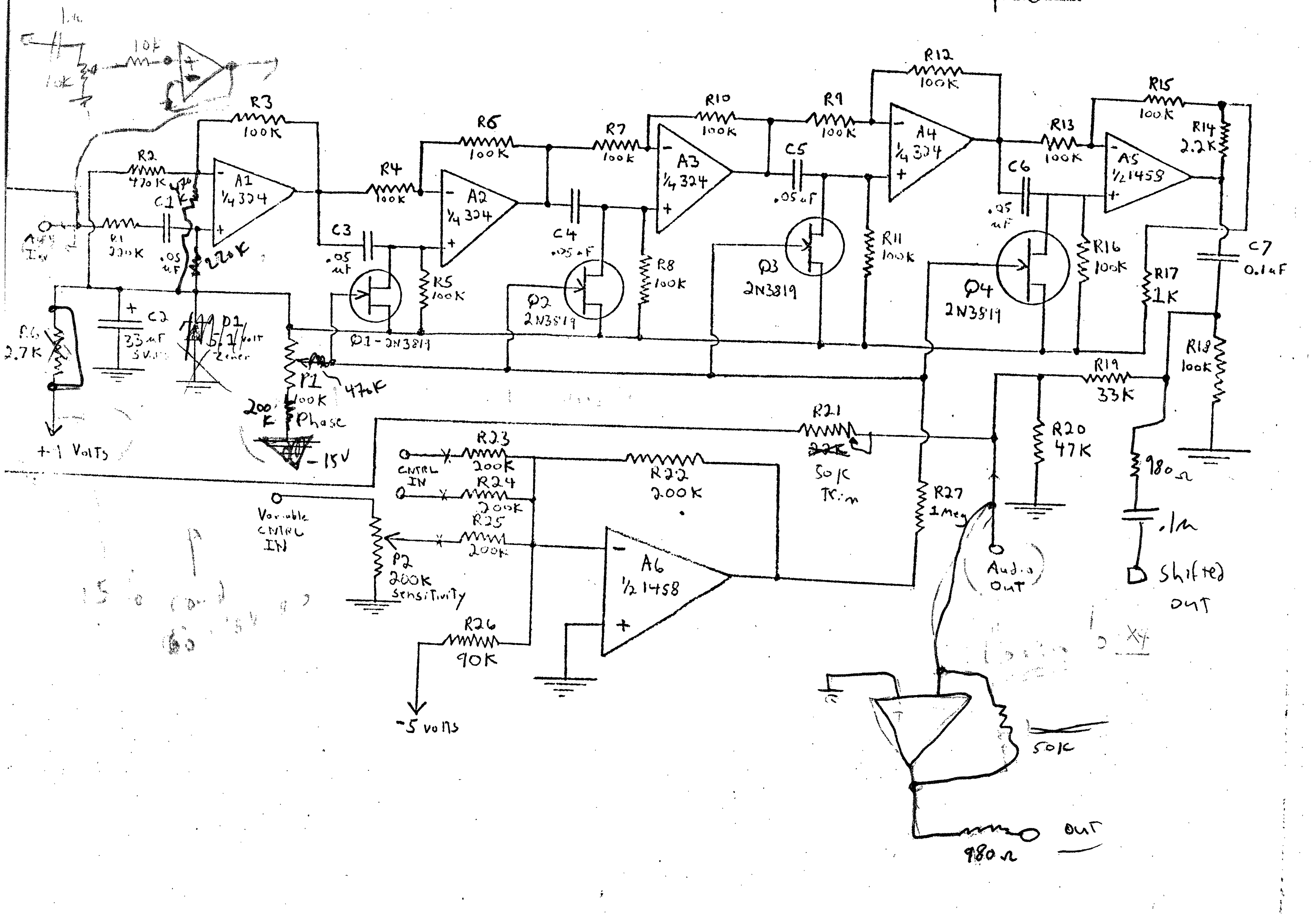
Inputs: Audio input
Phase control (fixed)
Phase control (variable)

Outputs: "Phased" audio output

Controls: P1 Phasing offset
P2 Variable phase control sensitivity

Uses: Simple FET controlled all-pass network shifts the phase of various frequency components with a control voltage. The "shifted" signal is mixed with the input, providing a "flanged" sound.

Phase Shifter



---Phase shifter---

The audio input to this circuit is AC coupled, and buffered through A1, then fed to the network A2-A5. Each amplifier in this network is built around a simple comstant amplitude phase lead circuit This type of circuit will pass all frequencies without attenuation (barring the natural roll-off of the OP-AMP), but vary phase by a selected amount determined in the shunt resistance from the '+' terminal to ground. Thus the paralell combination of R5, R8, R11, and R16 with the dynamic impedances of FET's Q1, Q2, Q3, and Q4 determine the amount of phase shift in each cell of the network. By varying the gate voltages of the FET's, we vary their impedance and thus shift phase. The gates are all tied together, and their bias is determined by P1 and the output of A6 (along with a negative bias to increase range), and this sum controls the shift in each cell of the network. Since the cells are cascaded together, the phase shifts are cumulative, and the total shift across the network is four times the shift of one cell alone. The original signal input is mixed with the phase-shifted output of the network via the impedance pad composed of R21, R20, R19, and R18, yielding a "flanged" interference sound at the audio output.

The original circuit ran form a unipolar nine volt supply, so zener D1 was added to bias the FET's and OP-AMP's. With a bipolar supply, D1 can be eliminated.

References:

The original design for this circuit was used by the MXR Corporation in thier "Micro-fazer".

18) SEVEN STAGE BINARY COUNTER

Inputs: Counter clock input
Counter re-set

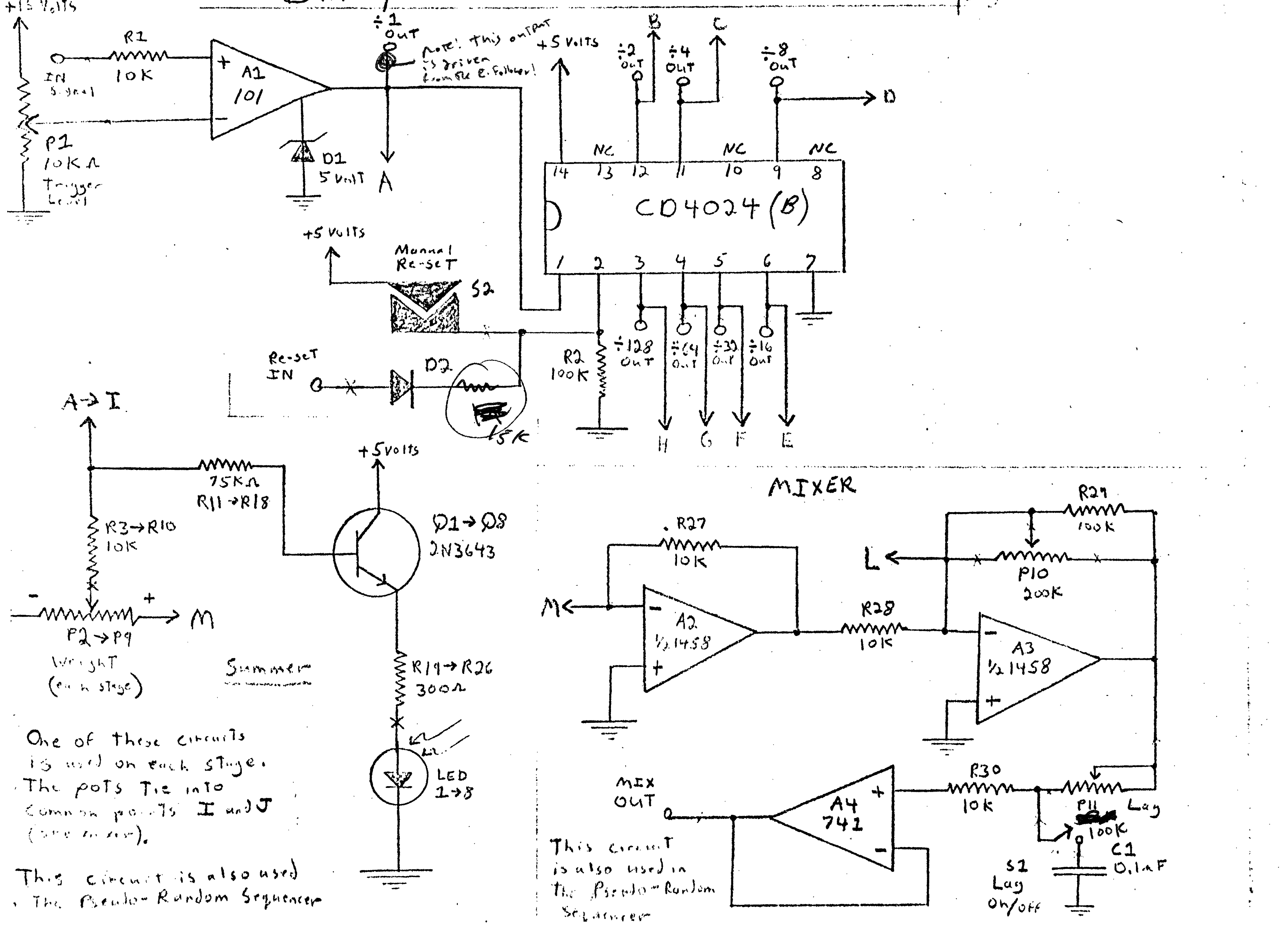
Outputs: Digital output of each stage
D/A sum of each stage

Controls: S1 Output Lag (LP filter -- ON/OFF)
S2 Manual counter re-set
P1 Input sensitivity (comparator threshold)
P2-P9 (+/-) mix weighting of each stage
P10 Master mix output gain
P11 Output Lag (amount)

LED's: LED1-LED8 One monitoring each stage (including input)

Uses: Can be used as a timer, sequencer, and frequency multiplier (with phase-locked loops). If it is driven by an audio source, it can provide subharmonics to enrich the tone. Digital inputs are comparator conditioned for analog compatability.

Binary Divider



One of these circuits is used on each stage. The pots Tie into common points I and J (see mixer).

This circuit is also used in The Pseudo-Random Sequencer

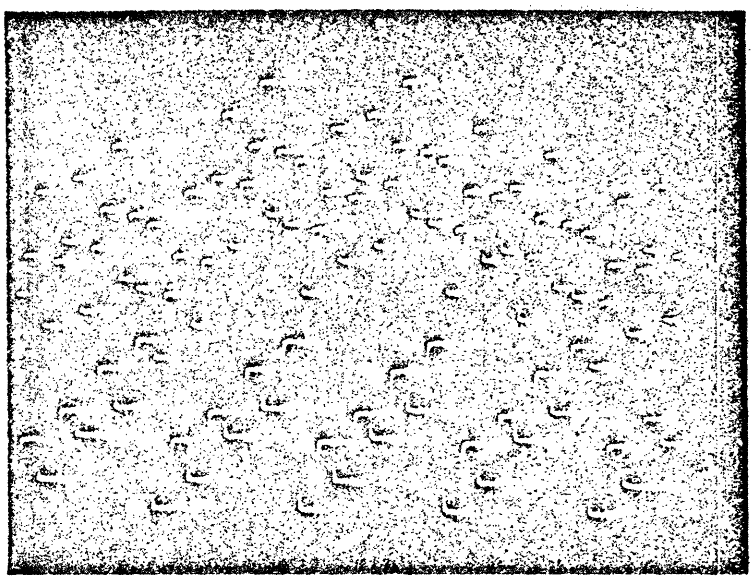
This circuit is also used in The Pseudo-Random Sequencer

---7 Stage binary Counter---

A1 is a comparator which compares the threshold voltage set on P1 at the '-' terminal with the signal input at the '+' terminal. This "squares off" the input waveform, and D1 clamps it to a 0-5 volt rectangular pulse. This pulse is input to the "summer" circuit, which buffers it via Q1 and activates monitor LED1. This circuit also weights the pulse via P2, and routes it to a mixing network composed of A2 and A3 with +/- inversion capability.

The original pulse is input to a CD4024 seven stage binary counter, which divides it into seven sub-octaves. The outputs of the counter are each input to a "summer" circuit, which drives a monitc LED and weights each stage in the A2/A3 mixer. The output of this mixer is passed through the transient-"lag" circuit, composed of P11, C1, and S1, buffered through voltage follower A4. The counter can be re-set by closing pushbutton S2, or by applying a positive voltage at D2.

References: NONE



Complex waveform produced by summing the stages of the divider

Simpler waveform so produced

Photo#30 - Waveforms produced on the binary divider

19) 9 STAGE PROGRAMMABLE/PSEUDO-RANDOM SEQUENCER

Inputs: Clock input
Ring counter re-set (stages 2-9)
External ring counter input (Xor'ed into feedback loop)

Outputs: Individual digital output of each stage of ring counter
Digitally conditioned clock input
A/D sum of each stage (variably +/- weighted)

Controls: S1* A/D output Lag (ON/OFF)
S1 Feedback mode (normal/inverted)
S2-S9 Feedback of each stage through Xor gates (ON/OFF)
P1 Clock input comparitor threshold voltage
P2 External ring counter input comparator threshold voltage
(P2-P10)* A/D weighting of each individual stage (+/-)
P10 - Master A/D mix gain
S10 - Manual ring counter re-set (stages 2-9)

* Denotes a circuit that appears on the Binary Divider schematic.

LED's: LED1 Clock monitor
LED2 External input monitor
(LED1-LED9)* Monitor on each ring counter stage

Uses: Can be used to provide a prognammable 1-9 stage control sequence. Can produce Pseudo-random pulse trains as long as 2**9 clock pulses. External counter input can be used to randomize and alter pseudo-random train. Can be chained to the 12 stage sequencer to provide programmable sequences up to 21 stages long. If driven by an audio source (clock), the sequencer can provide interesting harmonic rich sounds and waveforms. All digital inputs are comparator conditioned

Pseudo-Random Sequencer

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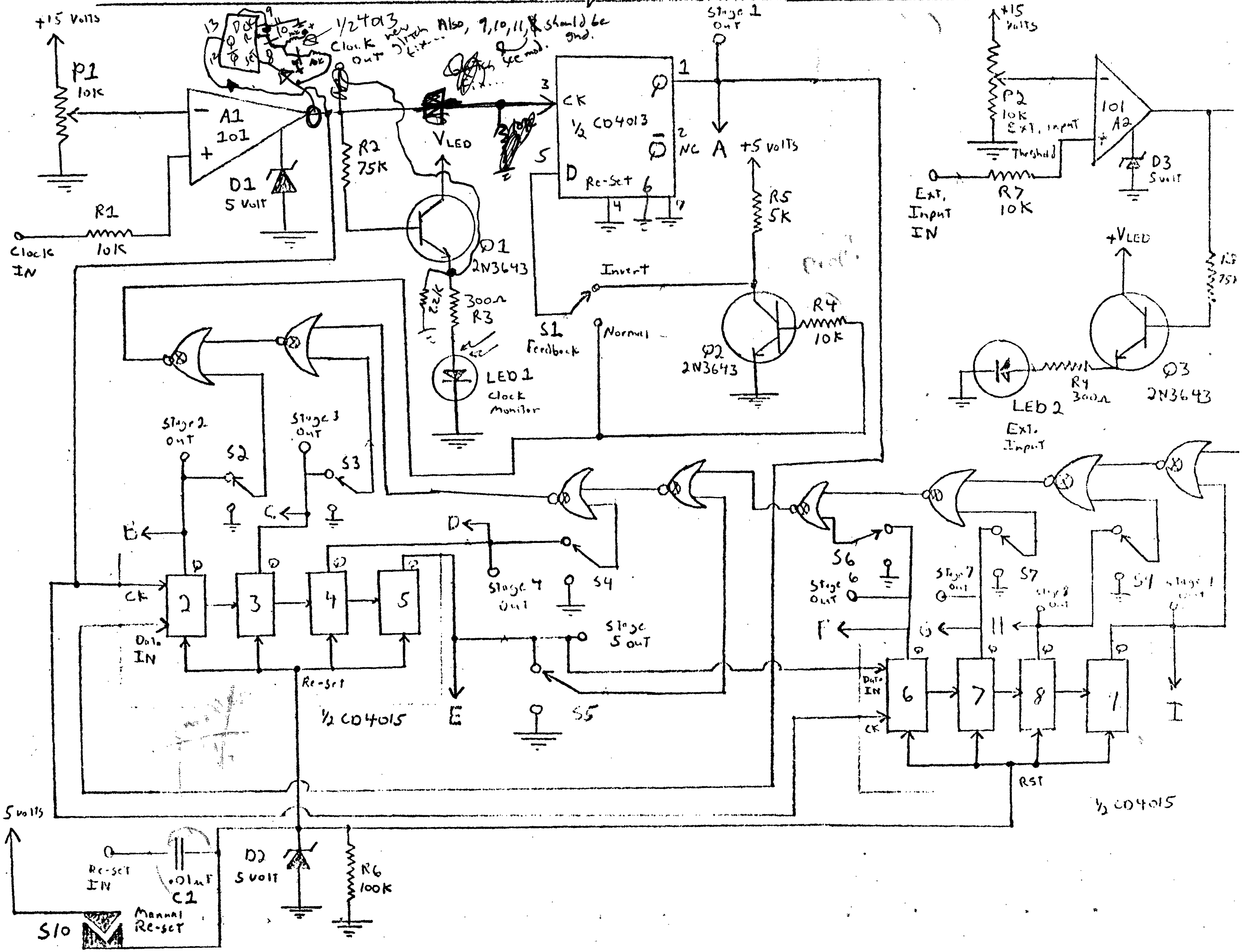
CD4030
Points A→I Tie To The "Summer" c...
(with The "Mixer" circuit) See The B... Divider Se...



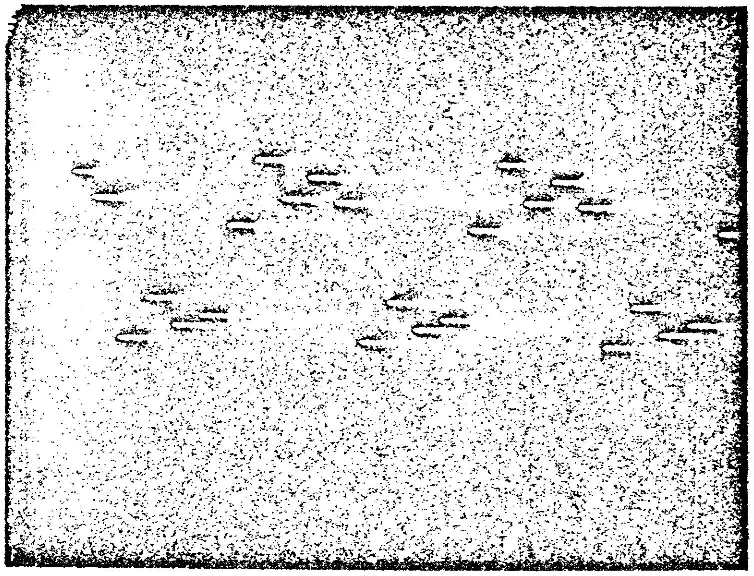
---9 Stage programmable/pseudo random sequencer---

The heart of this circuit is a nine stage digital ring counter. The first stage is composed of a CD4013 "D" flipflop. This is tied to two serial four-stage shift registers contained within a CD4015 package. Each stage can be optionally fed-back to the input of the first stage via an external switch (S2-S9) which routes the channel output into a chain of exclusive OR gates (the CD4030 is used). This allows one to set pseudo-random sequences of varying lenth. An external input is conditioned by comparator A2 (threshold set by P2) and clamped by D3. This imput is exclusive OR'ed into the feedback train, and it allows one to dynamically alter the pattern locked in the ring counter. The counter is clocked by a signal conditioned by comparator A1 (threshold set by P1), and clamped by D1. Both the clock and external inputs drive monitor LED's via buffers Q1 and Q3. The counter may be re-set by depressing S10 or applying a pulse at the re-set input (protected by D2). The re-set only zeroes the CD4015 (stages 2-9), and leaves the CD4013 (first stage) untouched. This allows one to program the sequencer for definite repeating patterns lasting from two to nine stages long.

Each counter output stage is routed to a "summer" circuit (see binary divider schematic. Points A-I are tied to summer circuits), where it drives a monitor LED and is weighted with inversion (+/-) capability in a "mixer" circuit. The sequencer also contains a conventional buffered RC transient lag at the mixer's output.

References:

"Pseudo-noise Timbre Generators", by Ralph Burhans. Journal of the Audio Engineering Society, April 1972



Photo#31 - A repeating sequence created on the nine stage sequencer

20) TRANSIENT LAG

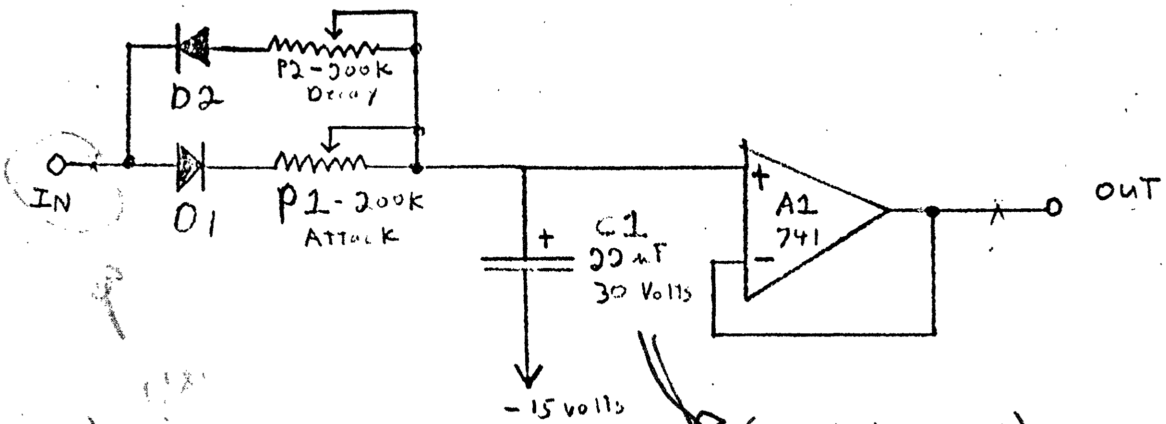
Inputs: Signal Input

Outputs: Signal output (through RC Lag)

Controls: P1 Attack lag time
P2 Decay lag time

Uses: Can be used to provide a variable Attack/Decay transient to a control signal. Also filters any unwanted noise from the signal input.

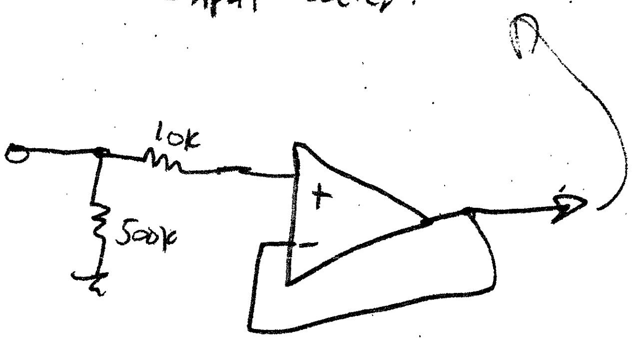
LAG



Switchable: 1) .1, 2.0, 22 µF

2) .68, 22 µF

Input Buffer:

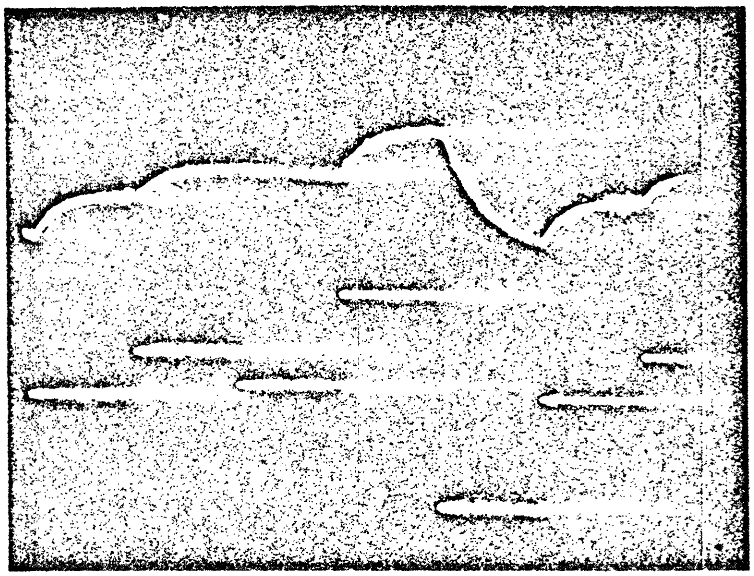


1/2 1458

--Transient Lag--

This circuit is straightforward. The input signal is fed to A1 via the low-pass filter composed of P1, P2, and C1. This gives the signal an exponential "lag". D1 and D2 seperate the charge-discharge paths of C1, thus the speed of attack is varied through P1, and the speed of decay is varied through P2. The voltage across C1 is buffered through voltage follower A1.

References: NONE



Output of Lag

Input waveform

Photo#32 - Lag transfer function

21) BALANCED (RING) MODULATOR

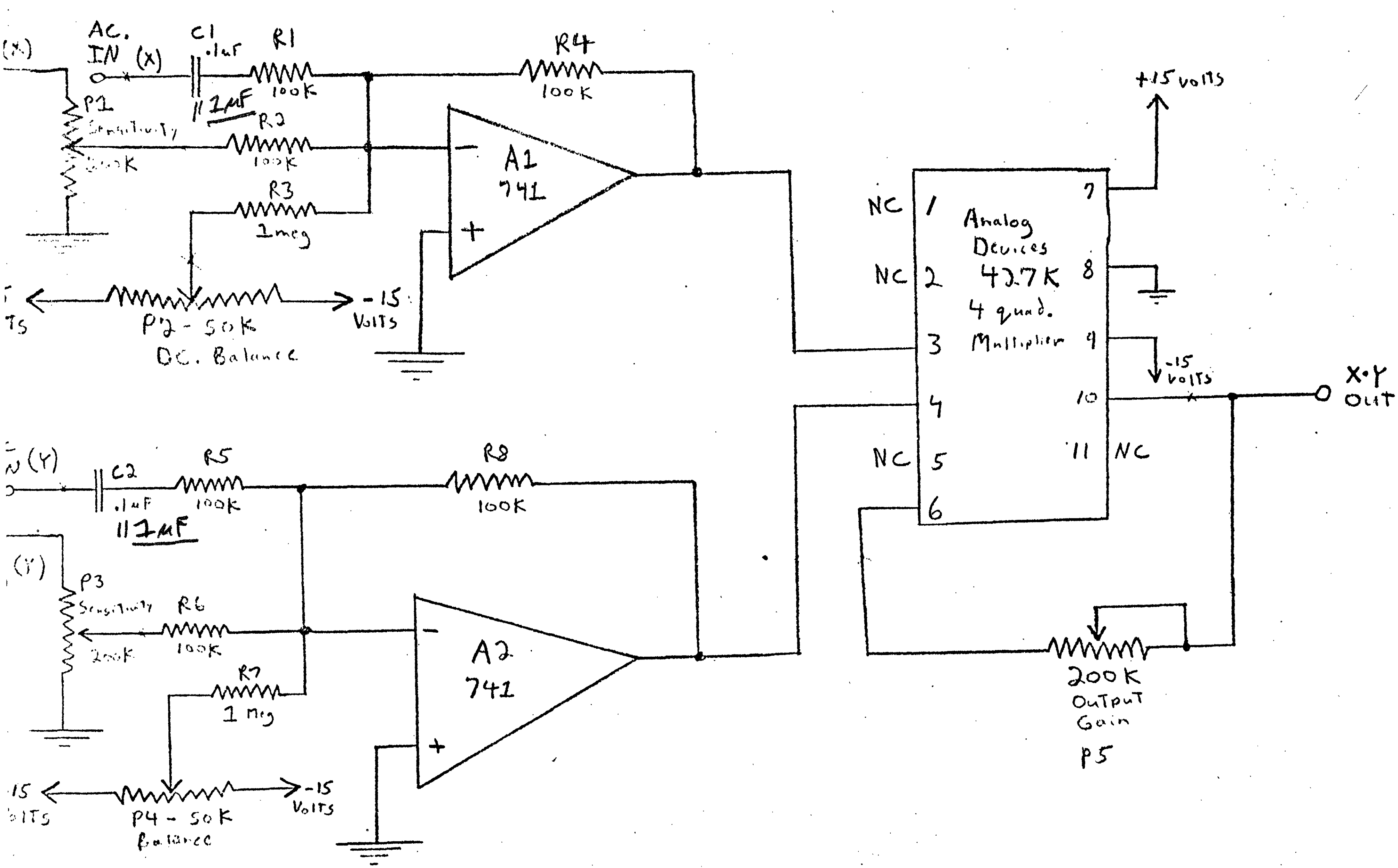
Inputs: X input (DC coupled)
X input (AC coupled)
Y input (DC coupled)
Y input (AC coupled)

Outputs: X*Y (4 quadrant multiplication)

Controls: P1 X DC input sensitivity
P2 Y DC input sensitivity
P3 X DC offset null
P4 Y DC offset null
P5 Multiplier output gain

Uses: Can be used to modulate two audio signals, providing familiar "bell" and "gong" effects. Also can be used to combine DC control signals. Uses an Analog Devices 427K high performance multiplier.

Ring Modulator



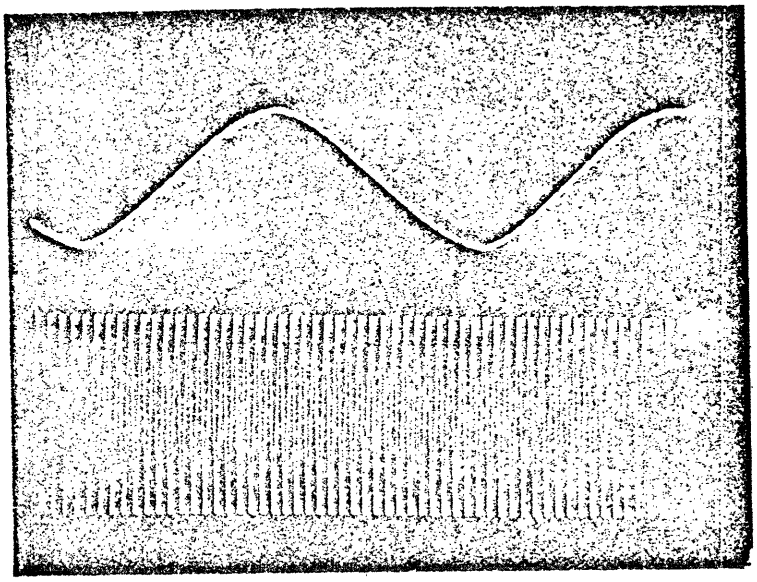
---Balanced (ring) modulator---

A1 and A2 are simple mixers which add an AC input coupled through C1 and C2, a DC input attenuated with P1 and P3, and a DC offset null set by P2 and P4. The resultant two outputs are fed into the X and Y channels of the 427K multiplier. This device performs multiplication by modulating the width of a high frequency pulse with the X input, and modulating its height with the Y input. The envelope of this conditioned pulse is proportional to the product of X and Y. P5 is a feedback potentiometer which adjusts the gain of the multiplier.

When the DC biases are nulled from the inputs via P2 and P4, the output of the multiplier will only contain the sum and difference frequencies of X and Y. All output will be composed of sidebands, and no original carrier will be transmitted through.

References:

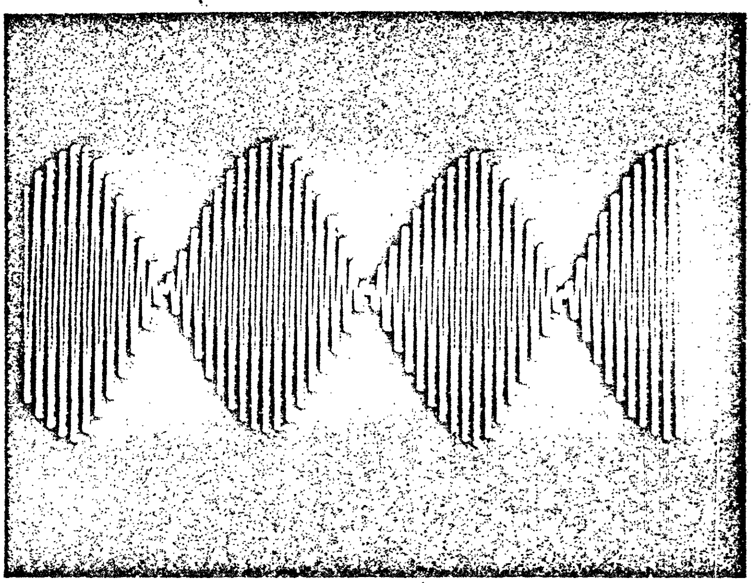
Analog Devices application notes



Sinosoid input to "X" input of modulator

Sinosoid input to "Y" input of modulator

Photo#33 - Modulator inputs



Photo#34 - X*Y Modulator output from the input above

22) DC/AC COUPLED VCA

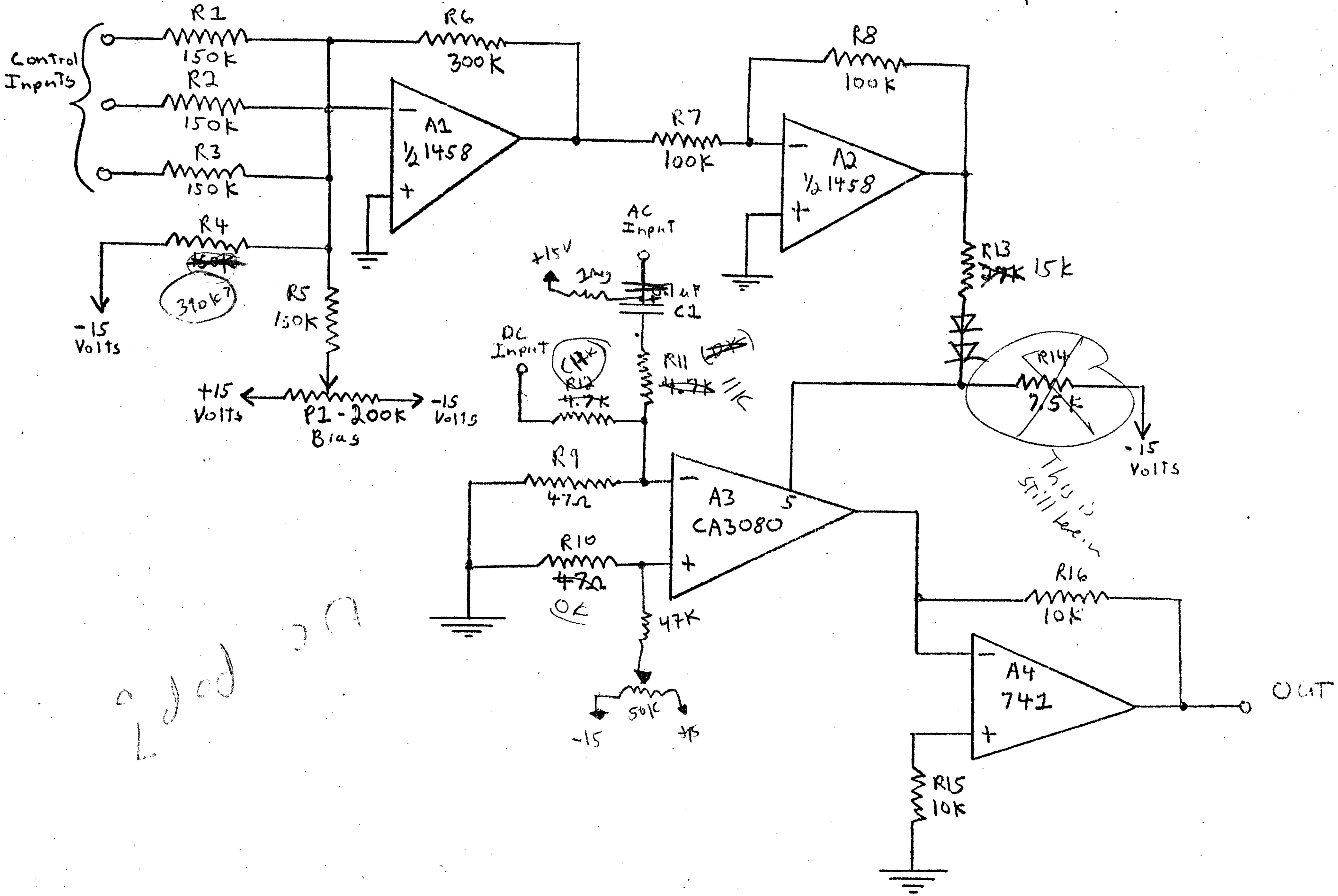
Inputs: Signal input (DC)
Signal input (AC)
Control input

Outputs: Signal output

Controls: P1 Control input bias

Uses: Can be used as an amplitude modulator for audio signals, or it can control DC control signals via analog gating. Uses the CA3080 transconductance amplifier.

VCA (With CA3080)



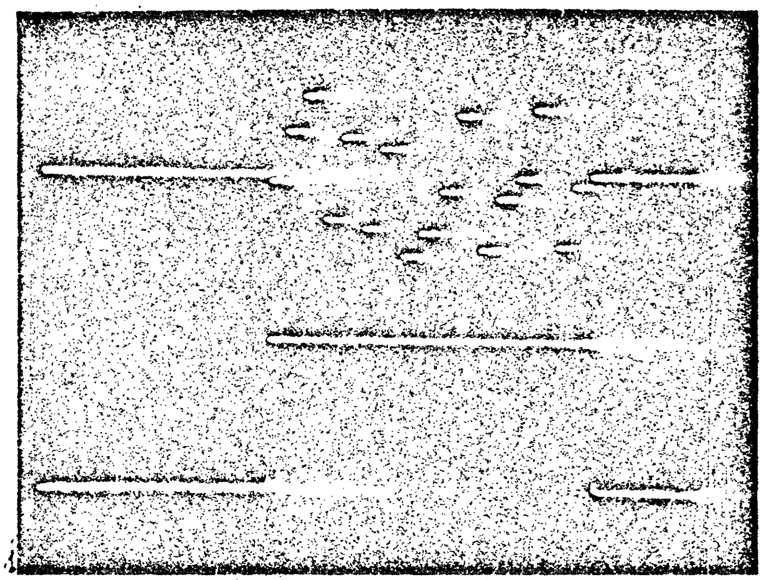
---DC/AC coupled VCA---

This circuit is centered around the CA3080 Operational Transconductance Amplifier (OTA for short). An AC coupled input (through C1) is mixed with a DC input via R11 and R12 at the input of OTA A3. Since the output of A3 is current-sourcing, it is passed through the current-to-voltage converter A4.

The gain of A3 is set by the current flowing into pin#5. This is determined by the output of summer A1/A2 (and the bias flowing through R14). The summer mixes the control inputs with a bias set by P1 and R4. The control inputs, then, effectively modulate the gain of A3. This device functions as a true two quadrant multiplier.

References:

Information on the CA3080 was located on page 453 of Walter K. Jung's IC OP-AMP Cookbook (Sam's Publications)



Output of VCA

Pulse fed to control
input of VCA

Photo#35 - VCA - (a complex step wave is input
to the VCA)

23) STATE VARIABLE VCF

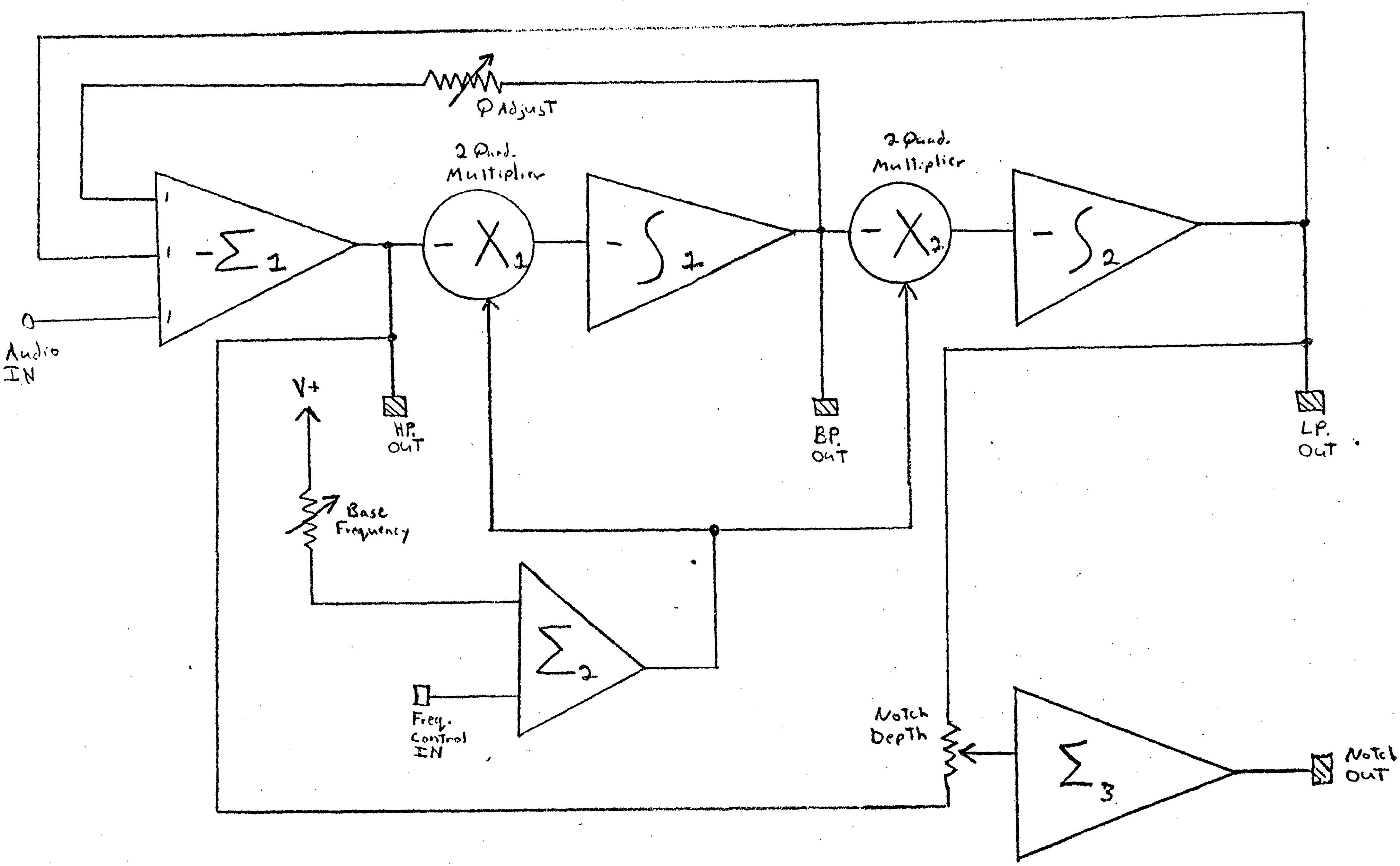
Inputs: Fixed audio in
Variable audio in
Fixed frequency control in
Variable Frequency control in

Outputs: High pass out
Low pass out
Band pass out
Notch out

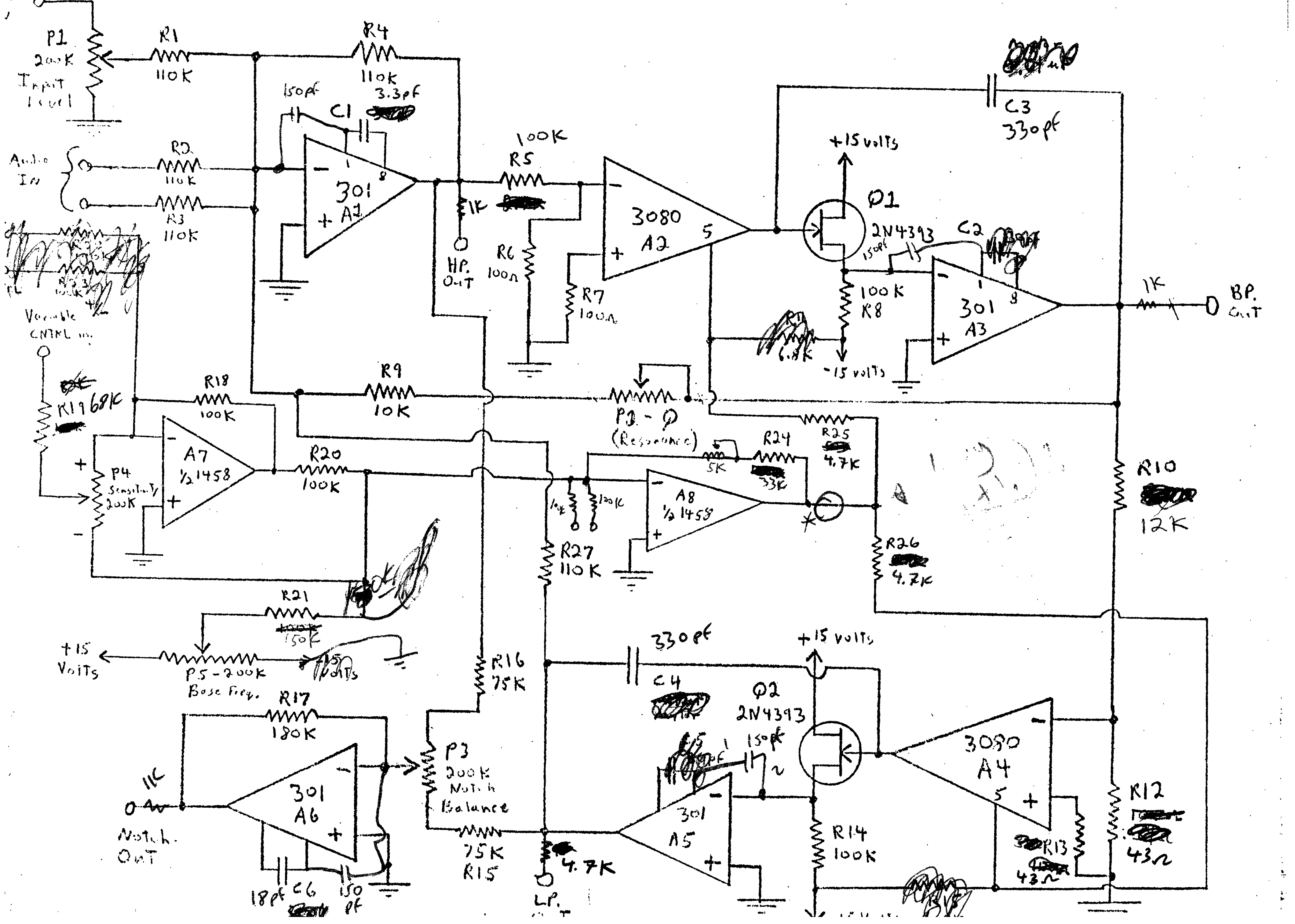
Controls: P1 Variable audio input level
P2 Resonance (Q)
P3 Notch balance
P4 Variable frequency control level (+/-)
P5 Center of "rest" frequency

Uses: High Q (possibly up to 500), High range (roughly 10 hz-20khz)
Used for dynamically altering the timbre of an audio signal.
Very popular and important element of the synthesizer.
Uses CA3080 OTA as a two quadrant multiplier.

State Variable VCF (block diagram)



State Variable Voltage Controlled Filter



---State Variable VCF---

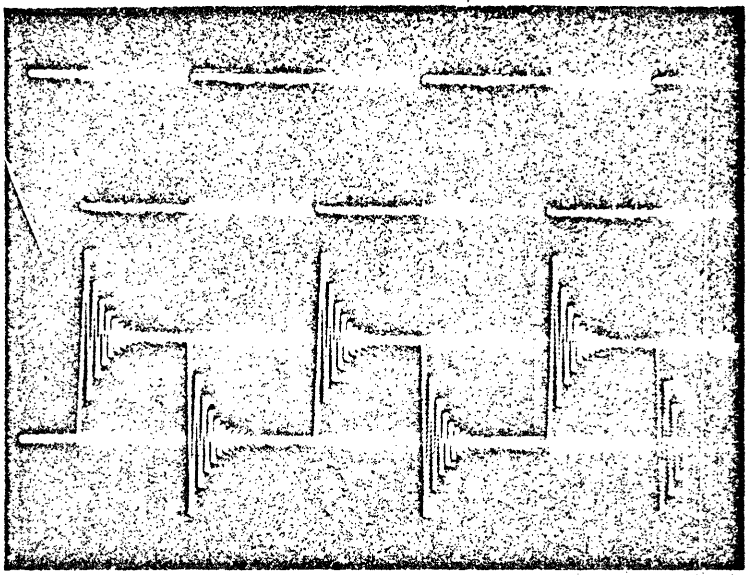
The block diagram shows the typical setup for a second order state-variable filter. The CA3080 chip is used as a multiplier between the integrators in order to voltage-control the center frequency. The controls are added with a bias determining the rest frequency set by P5 in summer#2 (A7/A8). One of the control inputs is variable with inversion (+/-) capability through P4.

The CA3080's are buffered by source followers Q1 and Q2 in order to reduce output impedance and bias problems (remember that the 3080's outputs are current sourcing!). The integrators incorporate the FET's into their feedback loops, thus linearizing them.

The high-pass and low-pass outputs are added together in summer#3 (A6), providing a notch response, with the balance of the notch set by P3.

References:

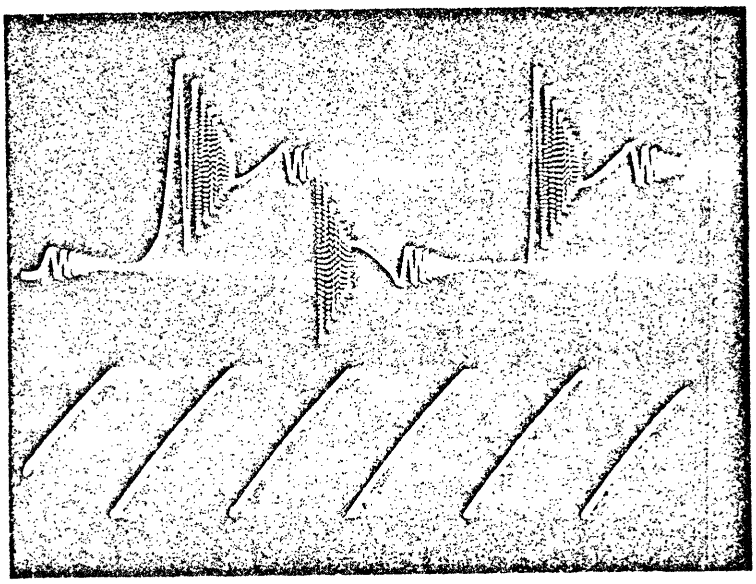
"Electrical design and Musical Applications of an Unconditionally Stable Combination Voltage controlled Filter/Resonator", by Dennis P. Colin
Journal of the Audio Engineering Society, December, 1971



Square wave audio input to VCF

Output of Low-pass with resonance added

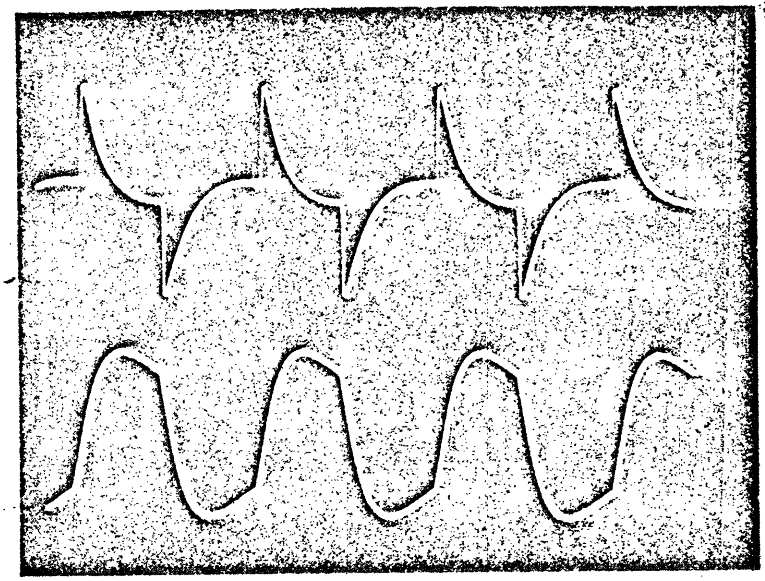
Photo#36 - Ring oscillation with resonance



Output of Low-pass (square wave is still input)

Linear ramp input to frequency control

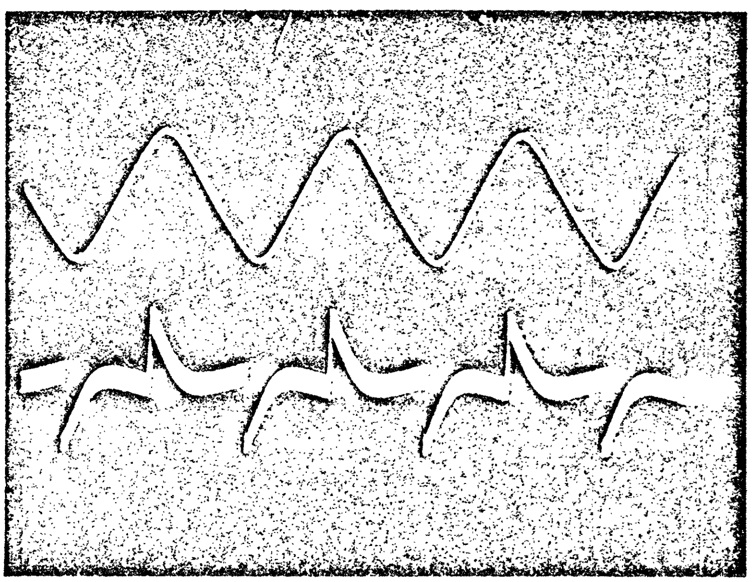
Photo#37 - Voltage control in the VCF



High Pass output

Band Pass output

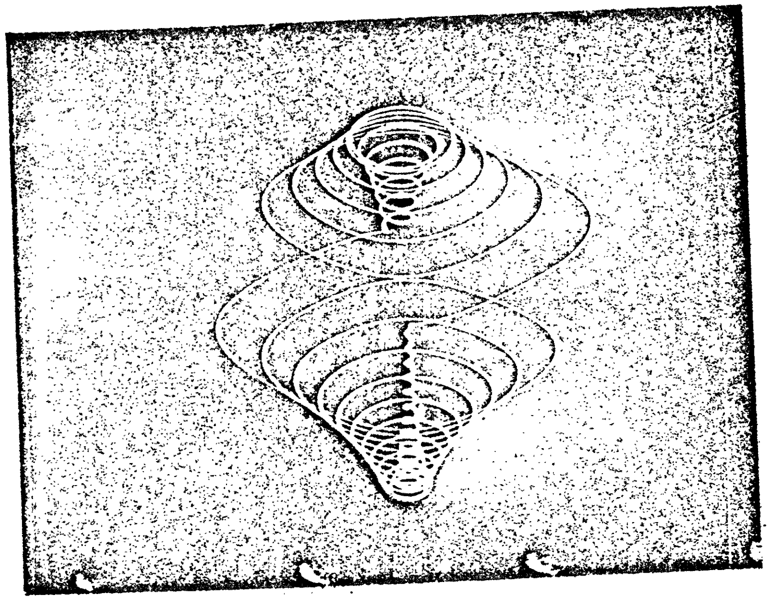
Filter waveforms without resonance
(input is still a square wave)
Photo#38



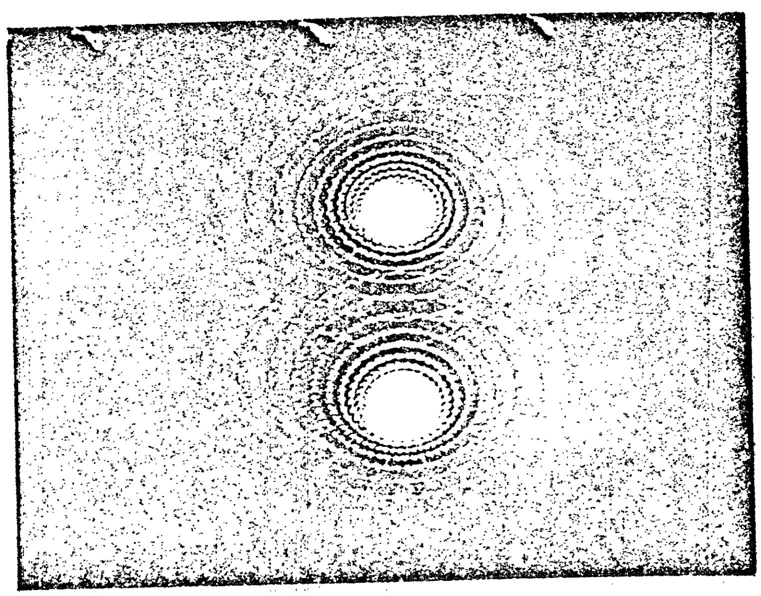
Low Pass output

Notch output

Photo#39 - Filter waveforms without resonance
(Square wave input)



Photo#40 - Crossplot of bandpass vs. lowpass outputs for a square/sine/triangle mix at the audio input



Photo#41 - crossplot of Bandpass vs. Lowpass outputs for a square wave audio input and a high frequency pulse added to the control input

24) EXTERNAL INTERFACE PROVISION

Inputs: External Audio Line 1 in , gain=4/3
External Audio Line 1 in , gain=20
External Audio Line 2 in , gain=4/3
Ecternal Audio Line 2 in , gain=20
External Pulse#1 in
External Pulse#2 in
Relay comparator trigger in

Outputs: Amplified Line 1 out
Amplified Line 2 out
Buffered pulse#1 out
Buffered pulse#2 out
Relay comparator out
External relay switch contacts

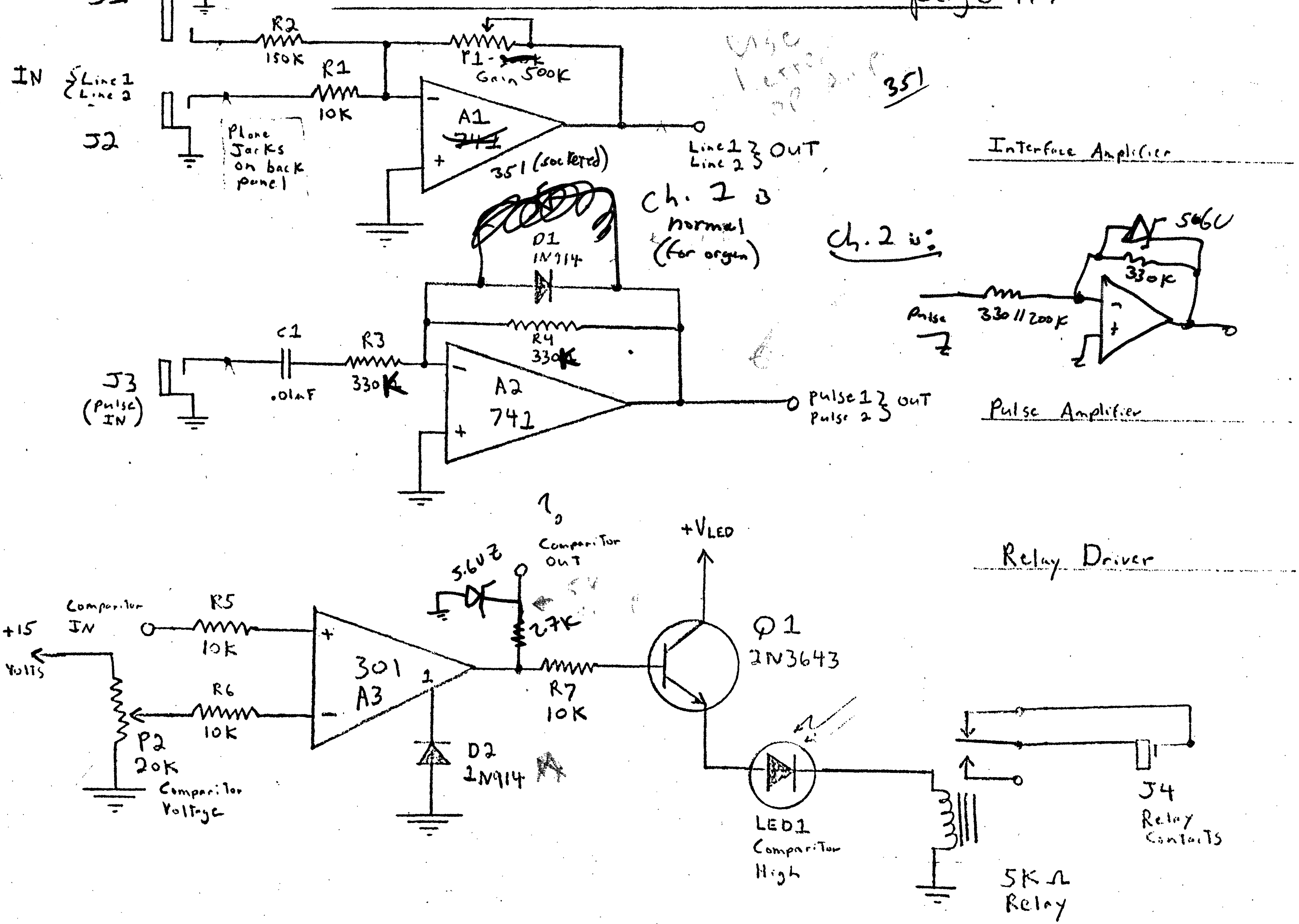
Controls: P1A Audio Line 1 gain
P1B Audio Line 2 gain
P2 Relay comparator threshold voltage

LED's: LED1 Relay triggered monitor

Uses: This module enables one to interface an external device to the synthesizer. 2 independent audio lines and 2 independent pulse lines are available. A comparator is included to fire a relay.

NOTE: The word "external" refers to an input or output which is only accessible through the rear interface panel.

INTERFACE


J1
IN {Line 1 / Line 2
J2
R2
150K
R1
10K
R1 - Gain 500K
A1
~~741~~
351 (socketed)
Phone Jacks on back panel
Line 1 / Line 2 } OUT
351
Interface Amplifier
Ch. 2 is normal (for organ)
Ch. 2 is:
560
330K
Pulse
330 // 200K
D1
1N914
C1
.01uF
R3
330K
R4
330K
A2
741
J3
(Pulse IN)
Pulse 1 / Pulse 2 } OUT
Pulse Amplifier
Comparitor OUT
5.6V Z
27K
+V LED
Relay Driver
Comparitor IN
+15 Volts
R5
10K
R6
10K
301
A3
P2
20K
Comparitor Voltage
D2
1N914
R7
10K
Q1
2N3643
LED1
Comparitor High
5K Ω Relay
J4
Relay Contacts

---External Interface provison--

Five seperate circuits are included in this package:

2 Interface amplifiers
2 Pulse amplifiers
1 Relay driver

The interface amplifiers are simple inverting summers with gain set by P1. These allow one to route external audio and control signals into the synthesizer. R1 (J2) gives a maximum gain of 20, and R2 (J1) gives a maximum gain of 4/3.

The pulse amplifiers AC couple to a trigger input via C1 (J3). The amplifier A2 is set for unity gain, and clamped positive by D1.

The relay driver is controlled by comparator A3, which compares an input against the threshold voltage set on P2. The output of the comparator is buought out and buffered by Q1,which drives the relay through monitor LED1.

All interfacing connectors are female phone jacks. All audio lines are shielded.

References: NONE

25) CREST/TROUGH DIODE MIXER

Inputs: Input A (crest)
Input B (crest)
Input A (trough)
Input B (trough)

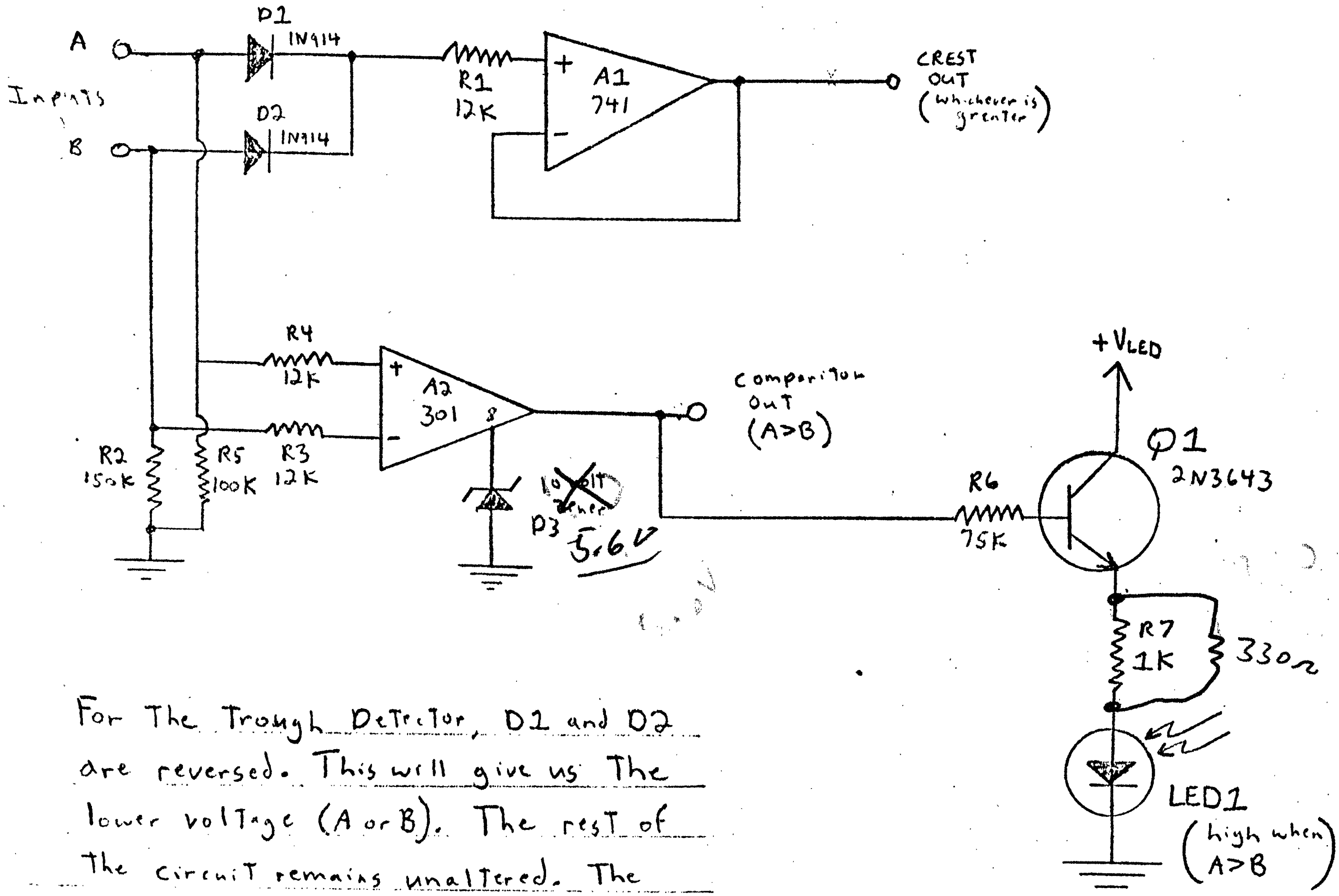
Outputs: Crest circuit...
Comparator - high when A.GT.B
Whichever input is greater, A or B
Trough circuit...
Comparator - high when A.GT.B
Whichever input is less, A or B

Controls: NONE

LED's: Two, one on each A.GT.B comparator (LED1 in diagram)

Uses: Interesting way to mix control signals, and the comparator output is very handy. When A and B are audio signals, very peculiar waveforms can be produced. Uses a simple buffered diode switch circuit.

CREST - TROUGH MIXER



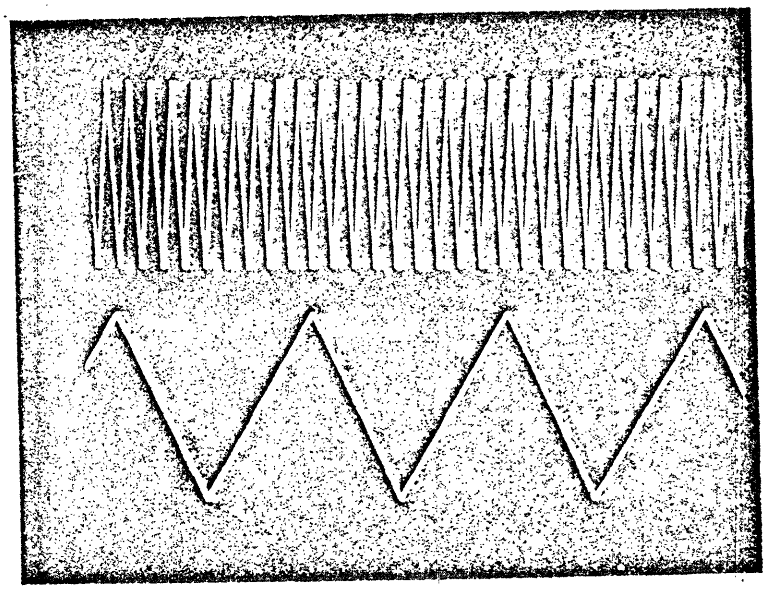
For The Trough Detector, D1 and D2 are reversed. This will give us The lower voltage (A or B). The rest of The circuiT remains unalTered. The ComparitoR sTill goes high when A>B.

---Diode Crest/trough mixer---

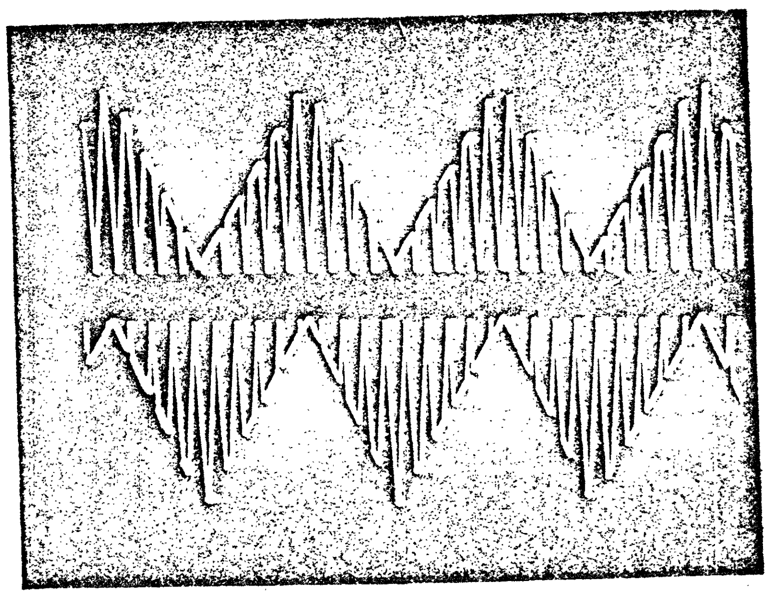
Whenever an input is applied at both A and B, diodes D1 and D2 present the greater voltage in the "crest" circuit, or the least voltage in the "trough" circuit, to voltage follower A1. A1 buffers this signal before it is output. A2 is a comparator which goes high when A is greater than B (D3 clamps it to 0-10 volts). The output of this comparator is buffered by Q1 and drives the LED.

R2 is greater than R5 inorder to keep comparator A2 low when no inputs are applied at A or B. The input bias currents cause a greater drop across R2, thus the comparator is held low in its quiescent state.

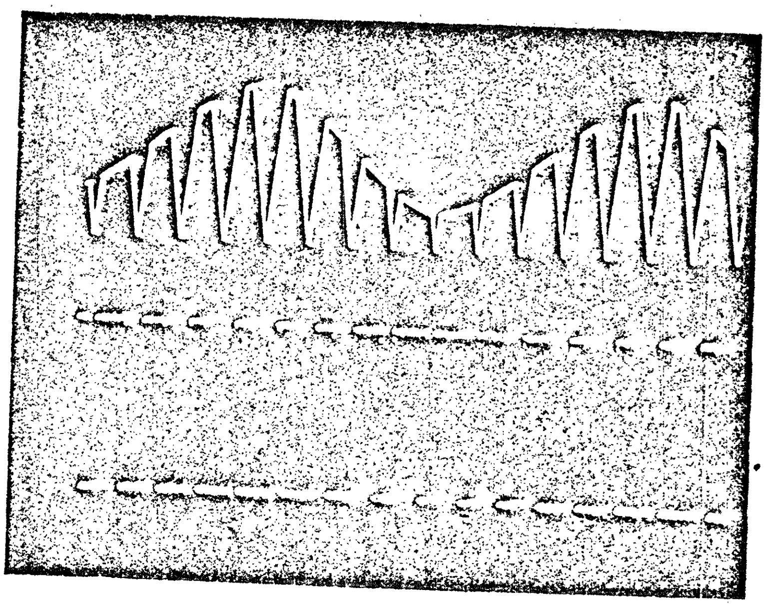
References: NONE



Photo#42 - waveforms input to the diode mixer to yield the output seen in photo#43



Photo#43 - outputs of diode mixer due to the above inputs



Crest output

A.GT.B Comparator
output

Photo#44 - diode mixer outputs (sine at 'A' , triangle at

26) TWELVE STAGE PROGRAMMABLE SEQUENCER

Inputs:	Run (clock runs when input high)	
	Synch (steps sequencer when in stop mode via external clock)	
	Clock frequency control	
	Ring counter load	
Outputs:	Digital output of each stage	
	A/D sum of variably weighted stages	
	Clock rectangular wave output	
	Clock pulse output	
Controls:	S1	Mode (Run/synch/stop)
	S2	Step ring counter manually (when in stop mode)
	S3	Load ring counter manually
	S4	Only one stage high at a time/several stages high simultaneously
	R134	A/D output RC lag (amount)
	R135	Clock frequency
	R136	Duty of clock rectangular wave
	----	Individual weight of each counter stage in A/D sum
LED's:	LED1-LED12	Monitor each ring counter stage
	LED13	Clock rate monitor
Uses:	Creates a programmable control sequence up to 12 stages long. Can be used with 9 stage sequencer to provide up to 21 stages.	

DESIGN ANALYSIS

CLOCK

As is shown in the block diagram of the sequencer (figure 7) and the schematic (figure 8), the clock does a lot more than simply provide timing pulses for the ring counter.

At the heart of the clock is a simple relaxation oscillator built around a single Norton amplifier stage (pins 1, 5 & 6 of IC-1) which is arranged in a Schmitt trigger configuration. Assuming that the RUN/STOP switch is in the "run" position, there are three major bias sources to the inputs of this amplifier. The first is into the non-inverting input (pin 1) through resistor R18. The second is also applied to the non-inverting input and is derived from the normally high output of the amplifier through R16. The third current flows into the inverting input through R34 as a result of the voltage that appears across the timing capacitor C4.

During the major portion of a clock cycle, the combined current flow into the non-inverting input of the amplifier exceeds that which flows into the inverting input and as a result the output of the amplifier is held very close to the positive supply voltage.

As C4 charges through the fixed resistance R35 and the front panel rate control R135 the voltage across it eventually becomes such that the resulting current flow through R34 exceeds the combined current flow of R18 and R16 and at this point the output of the amplifier switches to a low state. Two things happen simultaneously. The current that was flowing through R16 is removed so that the current through R34 will have to decrease significantly before the amplifier can switch again and diode D1 becomes forward biased and begins to discharge C4.

As C4 discharges, its voltage soon reaches the point at which the current through R34 is less than that through R18 causing the amplifier's output to once again switch high. This simultaneously reverse biases D1 and re-establishes the feed-back current through R16. From this point the cycle repeats.

The minimum width of the negative going clock pulses that appear at pin 5 of IC-1 is limited by the dynamic impedance of diode D1 and while they are relatively short (about 1% of the total period at the slowest clock rate) they are far too long to use directly on the clock line. The clock pulses are differentiated by C1 and R15 and used to switch a second amplifier section of IC-1 (pins 10, 11, and 12). The output of this amplifier stage is once again high riding with micro-second range pulses to ground.

Switching the RUN/STOP switch to the "stop" position introduces a fourth bias current to the amplifier in the relaxation oscillator by raising the ungrounded side of R30 to the positive supply voltage. The resulting current flow through R31 and R19 is such that the total current flow into the non-inverting input of the amplifier is much greater than the current produced by the highest voltage that C4 can charge to. The output of the amplifier cannot switch to its low state and the clock can be considered off.

The fourth bias current can be removed and the clock started either by returning S1 to the "run" position or by turning on transistor Q2, thereby shorting the junction of R19 and R31 to ground. Q2 can be turned on and held on by applying a positive voltage to the "run" input jack on the front panel or it can be turned on for very short periods of time for synchronization purposes by applying pulses to the "synch" input pin jack. Pulses applied to the "synch" input are differentiated by capacitor C3 with the negative going spikes at the trailing edges of the pulses clamped to ground by D2.

To examine the operation of this comparator, assume that the relaxation oscillator is at the point where it is just ready to fire and produce a clock pulse. At this point the output of the comparator is low because there is greater current flow into pin 3 than pin 2. As soon as the output of the relaxation oscillator (pin 5) goes low the current that was flowing through R39 is removed. Without the current contribution of R39, there is greater current flow into the non-inverting input than the inverting input and the output of the comparator switches to its high state causing a voltage step to appear at the step trigger output.

The output of the relaxation oscillator quickly returns to its normal high state; but at the time that it does, the voltage appearing across C4 is considerably lower than it was at the point of firing. Even through the current flow through R39 is restored, there is still greater current flow into pin 2 of the comparator than pin 3 because of the reduced current flow through R38. As the voltage across C4 increases, the point is eventually reached at which the currents through R38 and R39 exceed that through R136 and the output of the comparator returns to its low state removing the voltage step

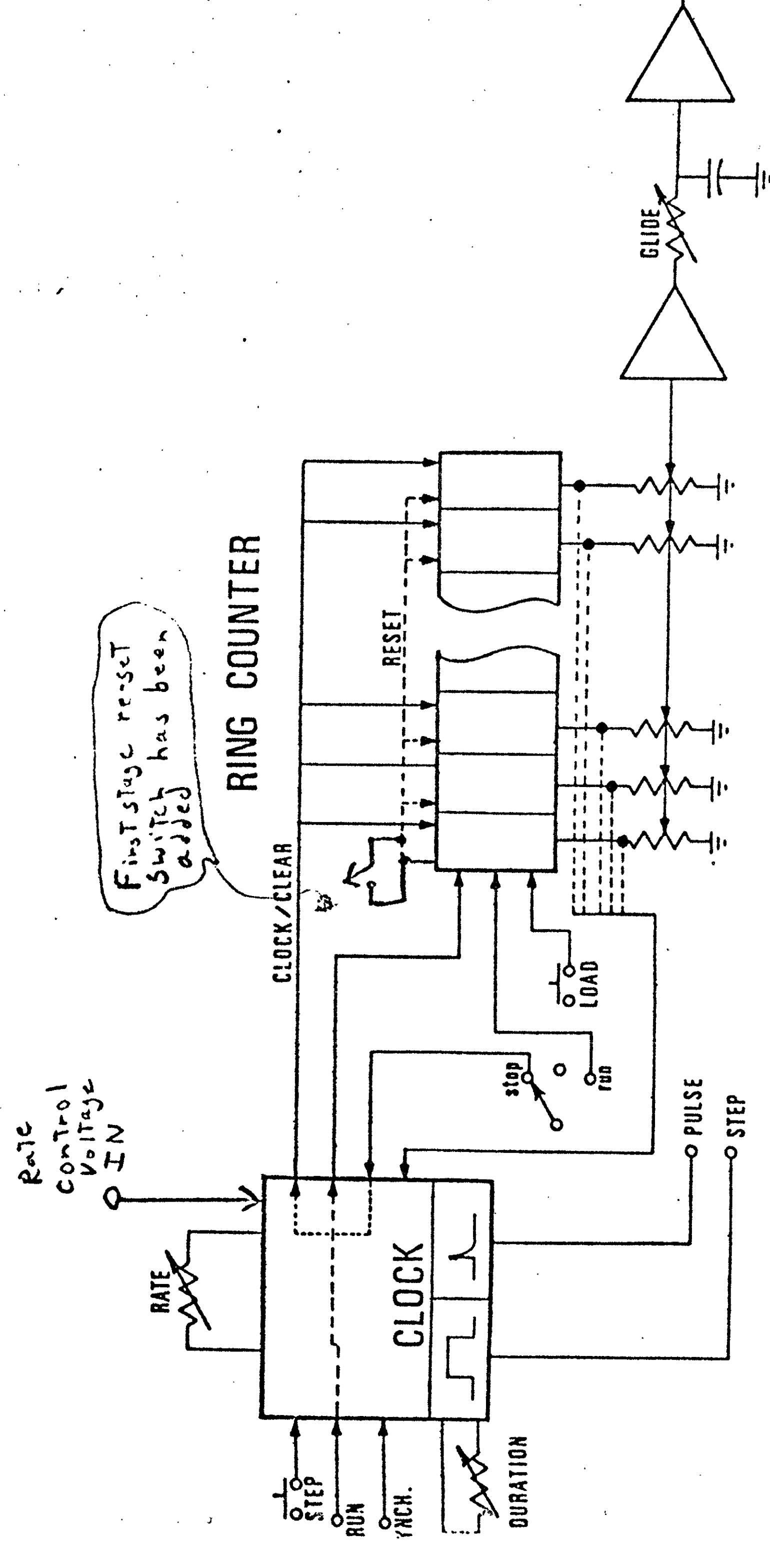


Figure 7

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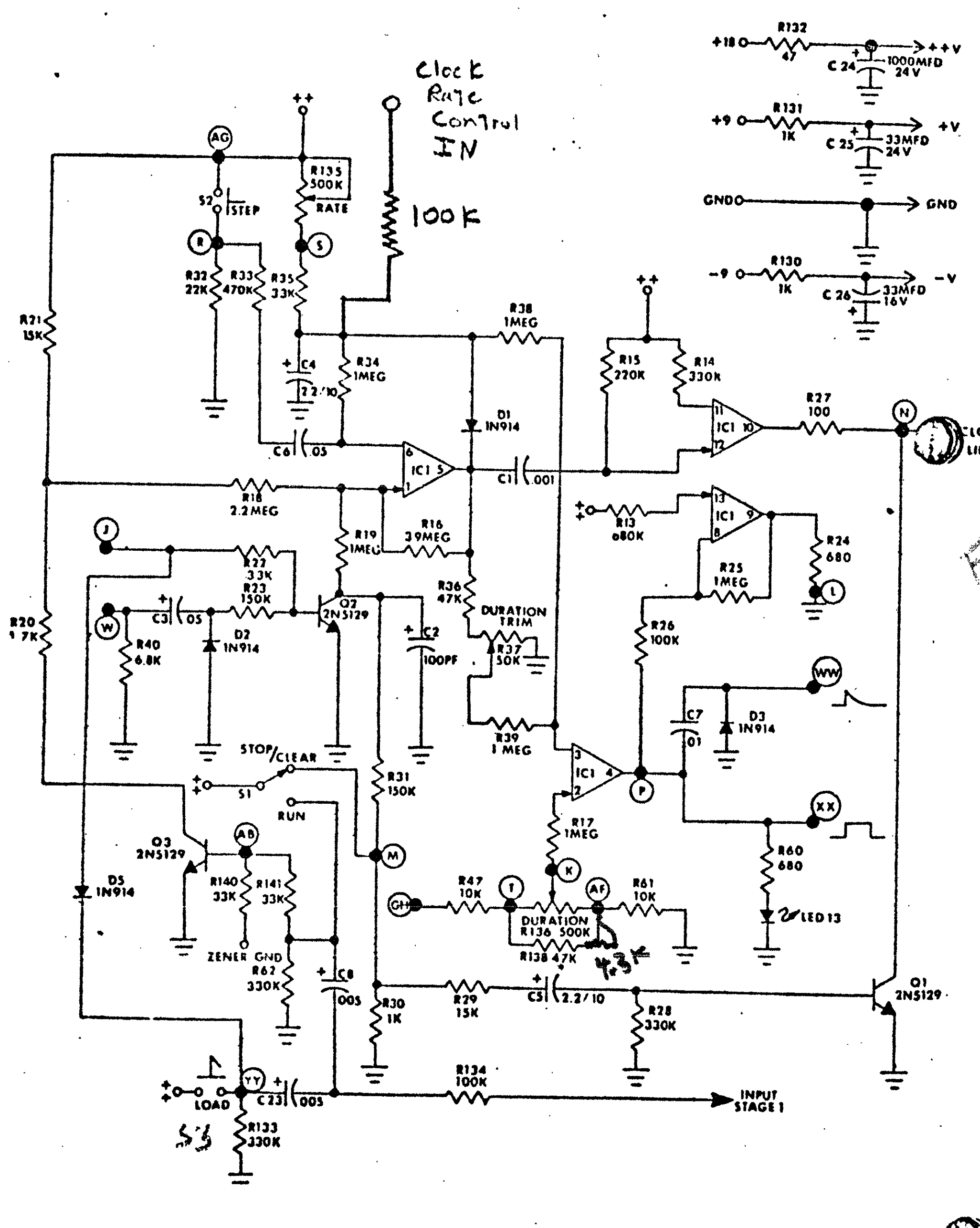


Figure 6

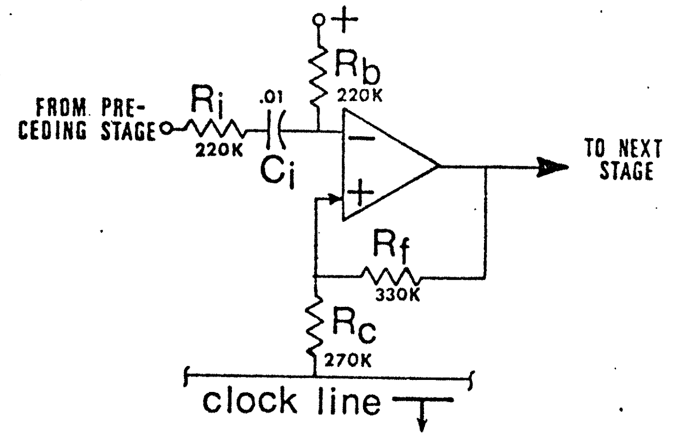
at the output. The point at which this transition to a low state occurs is a function of how high voltage across C4 has to rise before the inverting input current exceeds the non-inverting inpu current and this in turn is dependent on the setting of the front panel DURATION control.

When the output of the comparator switches high, the leading edge of the step is differentiated a pulse by C7 and appears at the front panel pulse trigger output jack. The negative spike that appear at the trailing edge of the step is clamped to ground by D3.

The step trigger also directly drives the light emitting diode LED-13 which indicates to the us duration of the step trigger output. In order to ease power supply regulation requirements, th relatively heavy periodic current flow required to light the LED is balanced by switching the d load R24 "on" anytime that the LED is off. The inversion required to perform this is provided the fourth stage of the amplifier in the IC-1 package, pins 8, 9 and 13.

RING COUNTER

The design of the ring counter section of the sequencer is a common concept employing 12 seri coupled latches. A typical stage is shown below. Like any other latch, this circuit has two st states. When the output voltage of the amplifier is low there is no current flow through the fee back resistor Rf and the greater current into the inverting input through Rb than through Rc int non-inverting input causes the output to stay low.



Once the circuit changes state to a high output a current begins to flow through Rf which when to the current already flowing through Rc results in a greater total flow into the non-inverting than is provided to the inverting input through Rb. The result is that the output stays high.

This stage can be "set" or "loaded" (output changed to a high state) by momentarily decreasing current flow into the inverting input. This is the case when the series capacitance and resist (Ri/Ci) are connected to the output of another latch whose output is transitioning from a high to low state. Once set, the stage can be reset by momentarily dropping the clock line from positi supply to ground.

If the time constant of Ri/Ci is chosen such that it is long when compared to the duration of the pulse, a ring of these stages will count by advancing the high state from one stage to the next e there is a clock pulse. In the process of being reset, each stage passes the count to the stage lately following it in the chain.

The entire chain can be cleared by holding the clock line at ground for a period of time greater the time constant of the Ri/Ci combination. When the RUN/STOP switch is set to the "stop/cle position, the series combination of R29 and C5 on the clock board generate a relatively long (. approximately) current pulse that turns on transistor Q1 which in turn shorts the clock line to

It is undesirable to have more than a single stage of the counter set at any given time, yet this situation would naturally occurr if the output of an intermediate stage of the counter was fed ba into the input. To prevent this, the output of stage one serves as a reset for the rest of the st

When stage one goes high, current supplied to the inverting inputs of the rest of the stages in the counter by way of R111 - R121 causes each stage to reset.

The first stage of the counter can be set in a variety of ways. Pressing the front panel LOAD push button causes a voltage to appear across R133 on the clock board which is coupled to the non- inverting input of the first counter stage by means of C23 and R134. Applying a voltage step to the front panel RUN input jack produces an identical result because of diode D5 (but note that pressing the LOAD button reverse biases D5 and will not cause the clock to run). Setting the RUN/STOP switch to the "run" position causes a voltage to appear across R62 which when coupled through C8 and R134 produces the same results.

Taking the first as typical, the output of each of the counter stages is connected through a current limiting resistor (R7) to a light emitting diode (LED-1). All of the LEDs in turn connect to a common line that returns to ground through the zener diode D4. These LEDs and the zener perform a number of functions.

First, the LEDs light to indicate to the user which stage is currently loaded. Second, the LED and zener together serve to clamp the voltage that appears across the voltage divider at the output of each stage (R41 in stage 1) to a reference level of approximately 6 volts and thereby assists in eliminating voltage drift at the control voltage output of the sequencer. Third, the LEDs function as normal diodes to prevent interaction between the twelve counter stages. Finally, the voltage that appears across the zener any time that any of the ring counter stages are set serves as a signal back to the clock that the counter is loaded.

The multi-turn potentiometers at the output of each stage of the counter are resistance coupled (R1 in stage 1) to a common line that feeds non-inverting summing amplifier IC-5. The output of the summing amplifier is connected to the glide circuit consisting of the front panel GLIDE control R137 and capacitor C22. The emitter follower Q4 serves as an output buffer to minimize unwanted control voltage level changes that could otherwise be a side effect of changing the glide rate.

In the "conditional run" (middle) setting of the clock's RUN/STOP switch, the clock runs only when there is a "1" loaded into the ring counter (see USING section). This is accomplished by using the voltage that appears across the zener diode D4 when any stage of the counter is high (see ring counter analysis) to turn on transistor Q3 on the clock board. As long as Q3 is on, the voltage divider R21 and R20 in the clock is connected between positive supply and ground causing a normal bias current to flow through R18. When Q3 turns off, the voltage divider is no longer grounded causing the junction of R21 and R20 to rise to essentially supply thereby forcing 4 times more current to flow through R18 than previously. As explained previously, this stops the action of the relaxation oscillator. When the RUN/STOP switch is in the "run" position the current to hold Q3 on is supplied through R141.

A third amplifier in IC 1 (pins 2, 3 and 4) takes care of generating the step and pulse trigger outputs of the sequencer. This amplifier is wired as a comparator so that its output voltage (at pin 4) is low until the sum of the currents into the non-inverting input through R38 and R39 falls below the level of the reference current through R136.

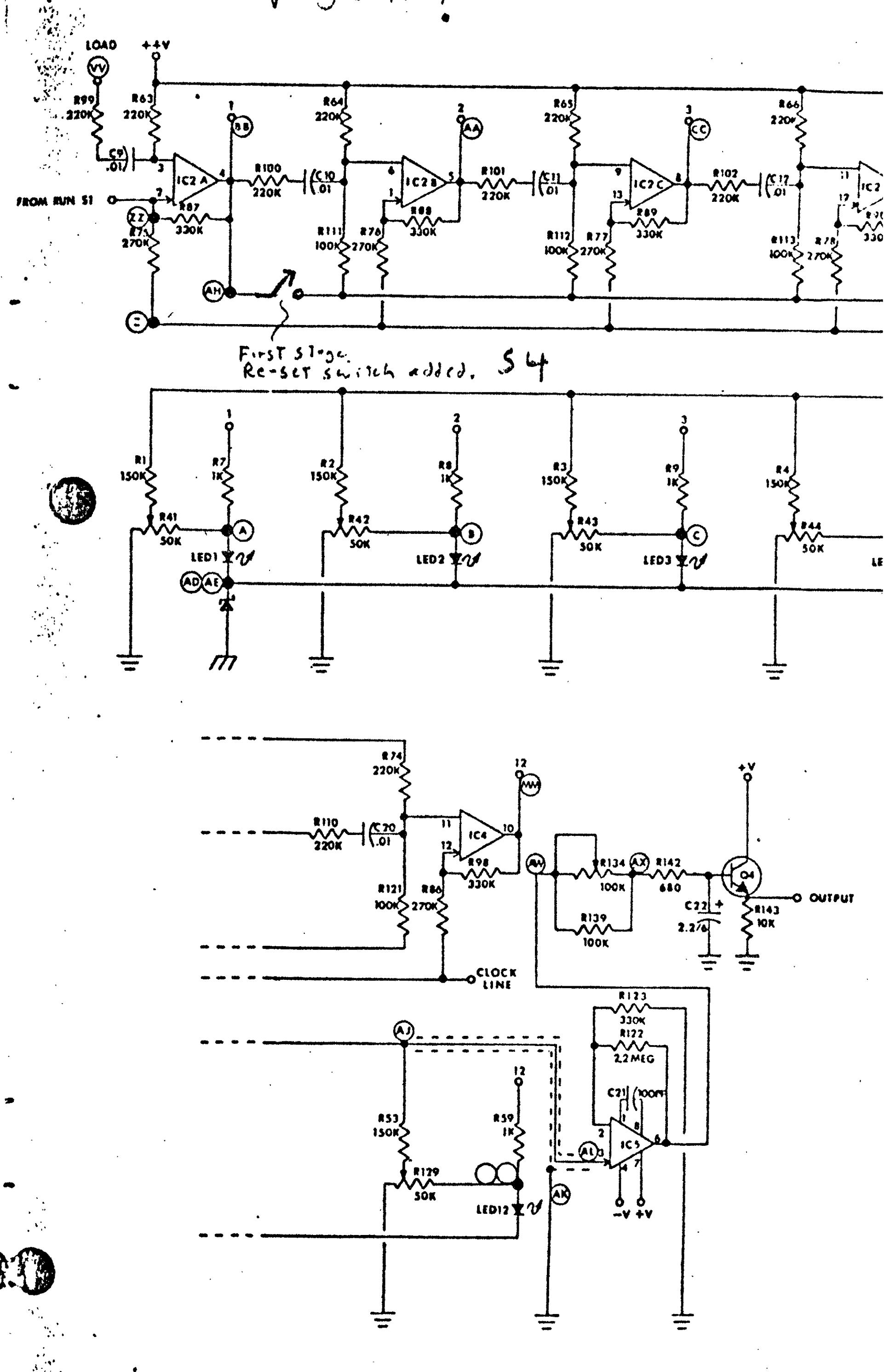


Figure 9

---12 stage programmable sequencer---

This circuit has not been altered substantially from its original design, so I have included modified original schematics, rather than composing new drawings. The circuit description is also included, so I won't go into detail here.

This sequencer is similar to the pseudo-random unit described earlier in that it is based around a ring counter. This unit contains its own clock, and I have installed a resistor to make it voltage controllable. (I have also installed a switch which enables more than one stage to go high at a time - S4.)

This module uses CDA's (LM3900) to simulate digital flip-flops. This can cause run-through problems in clocking. The earlier CMOS design is vastly superior in these respects, and its pseudo-random capability makes it more versatile. The two sequencers may be chained together to generate programmable sequences up to 21 stages long.

References: Basic Module is designed by PAIA electronics

27) QUAD 4 CHANNEL MIXER

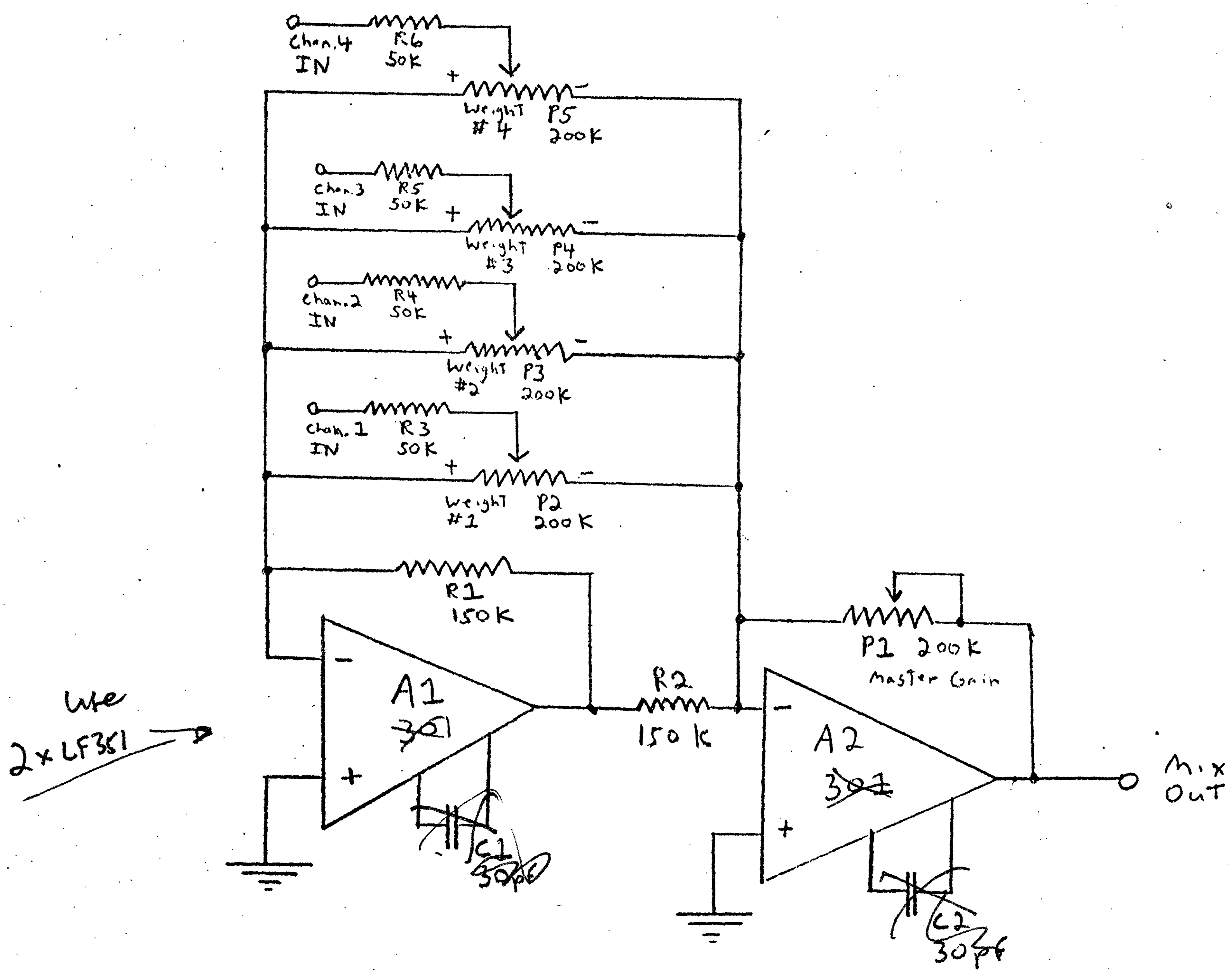
Inputs: 4 signal inputs per mixer

Outputs: Weighted sum of each input

Controls: P1 Master mix gain
P2-P5 Level with inversion (+/-) for each input

Uses: Used as a general purpose Audio/Control mixer. Inversion capability is handy.

4-Channel Mixer (with inversion capability)



---Quad 4 channel mixer---

There are four of these circuits in this module. This dual amplifier mixer is used widely throughout the synthesizer. Four inputs are scaled by P2-P5, and routed to either A1 (non-invert), or A2 (invert). P1 is a master control that sets the gain for all four channels. All inputs are DC coupled.

References: NONE

28) VOLTAGE CONTROLLED PAN

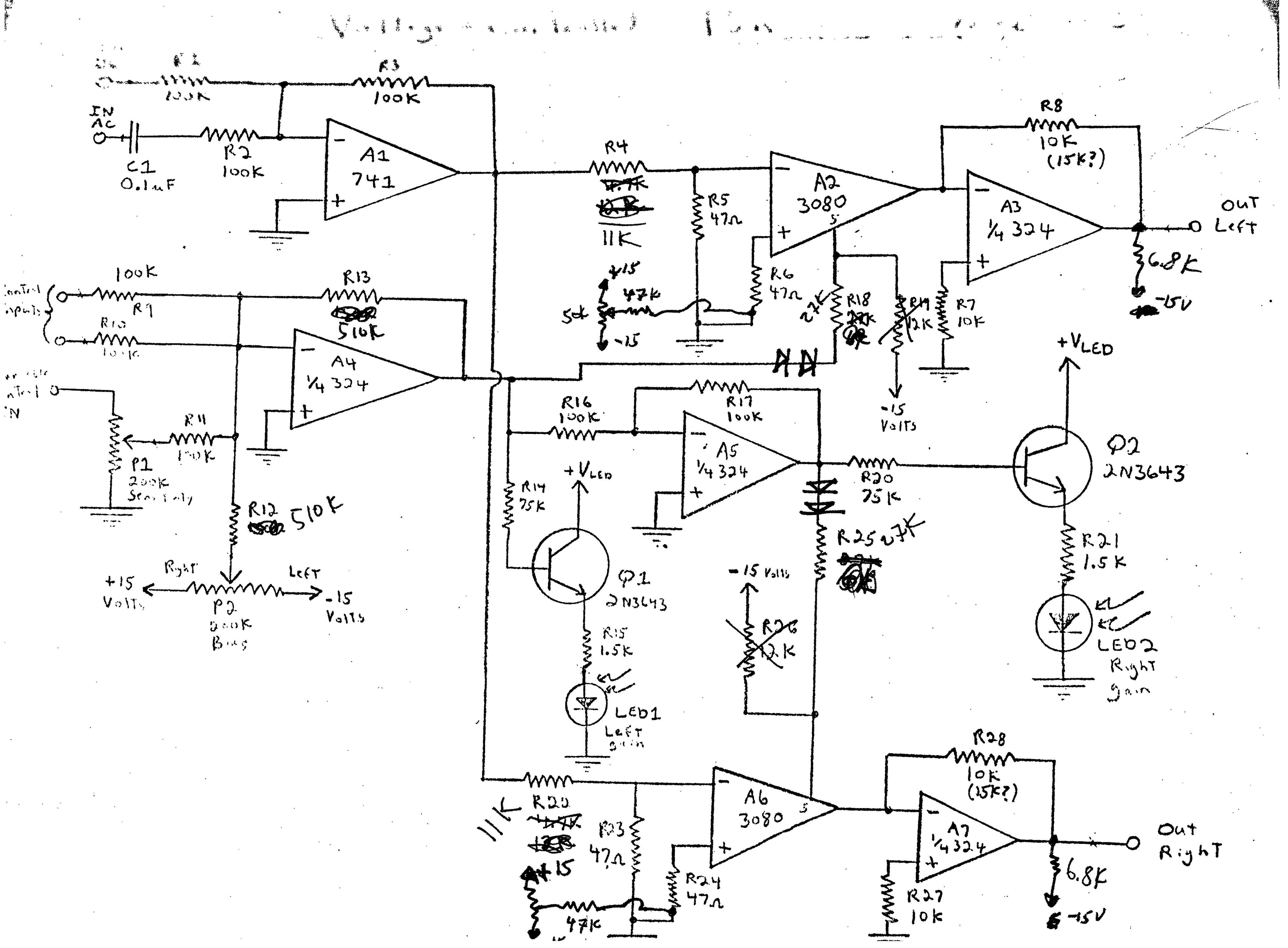
Inputs: AC coupled Input
DC coupled Input
Fixed position control input
Variable position control input

Outputs: Left channel out
Right channel out

Controls: P1 Variable position control sensitivity
P2 Position (Right/Left) Bias

LED's: LED1 Right channel gain monitor
LED2 Left channel gain monitor

Uses: This module routes an input to the right or left output, depending upon the magnitude and polarity of the input contro voltage. It can be used to "sweep" or "pan" an audio signal between stereo speakers, or it can route a DC control signal selectively to two destinations.



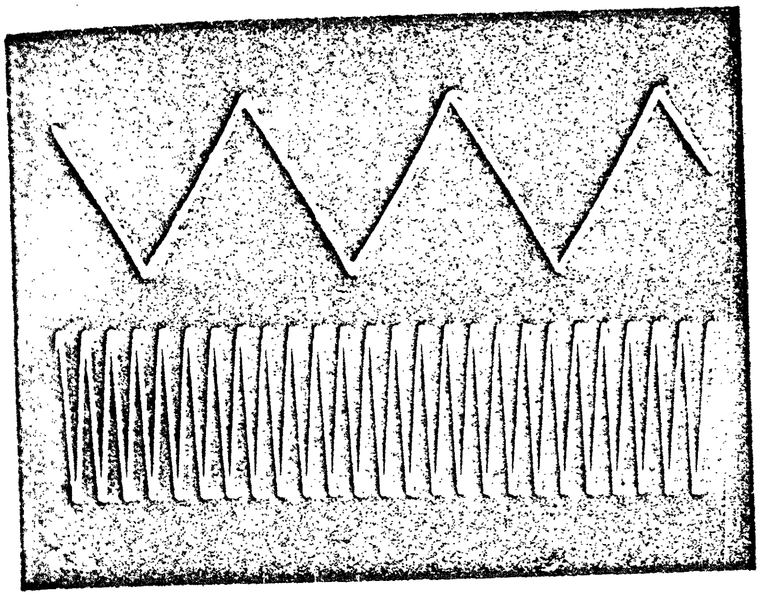
IN AC
C1 0.1uF
R2 100K
R3 100K
A1 741
R4 11K
R5 47Ω
A2 3080
A3 1/4 324
R8 10K (15K?)
OUT Left
6.8K
-15V
R6 47Ω
R18
R19 2K
R7 10K
-15 Volts
+15
47K
Set
-15
100K
R1
R10
R13 510K
A4 1/4 324
R11 100K
P1 200K
R12 510K
Right
Left
+15 Volts
-15 Volts
P2 200K Bias
R16 100K
R17 100K
A5 1/4 324
R14 75K
+VLED
Q1 2N3643
R15 1.5K
LED1 Left
R20 75K
Q2 2N3643
+VLED
R25 27K
-15 Volts
R26 2K
R21 1.5K
LED2 Right
R22 11K
R23 47Ω
+15
47K
R24 47Ω
A6 3080
R28 10K (15K?)
A7 1/4 324
R27 10K
6.8K
-15V
Out Right

---Voltage controlled Pan---

The DC and AC inputs (coupled via C1) are mixed in unity gain summer A1. The output of A1 feeds the inputs of two CA3080 transconductance amplifiers, A2 and A6, which drive current-to-voltage converters A3 and A7. The control input signals are mixed with the bias set via P2 in A4. The output of A4 is fed to pin#5 of A2, determining the left channel gain. This signal is inverted in A5 and fed to pin#5 of A6, determining the right channel gain. We now have a situation where the gain of one channel is inversely proportional to the gain of the other. Thus we can "pan" an input back and forth from right to left with a control voltage.

The right and left control voltages are buffered via Q1 and Q2, and fed to the LED's, giving us a monitor on the gain of each channel.

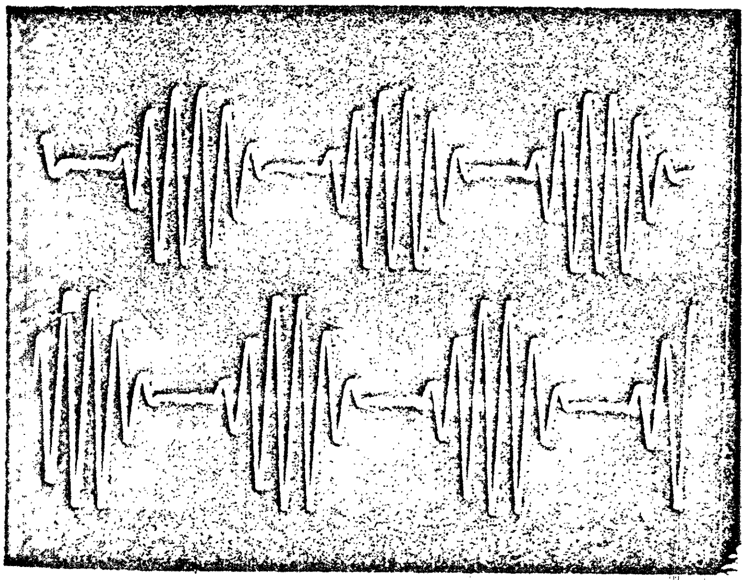
References: NONE



Wave fed to control input of VCP

Wave fed to audio input of VCP

Photo#45 - waveforms input on the voltage controlled pan



Left channel output

Right channel output

Photo#46 - outputs of VCP with the input shown above

29) AGC

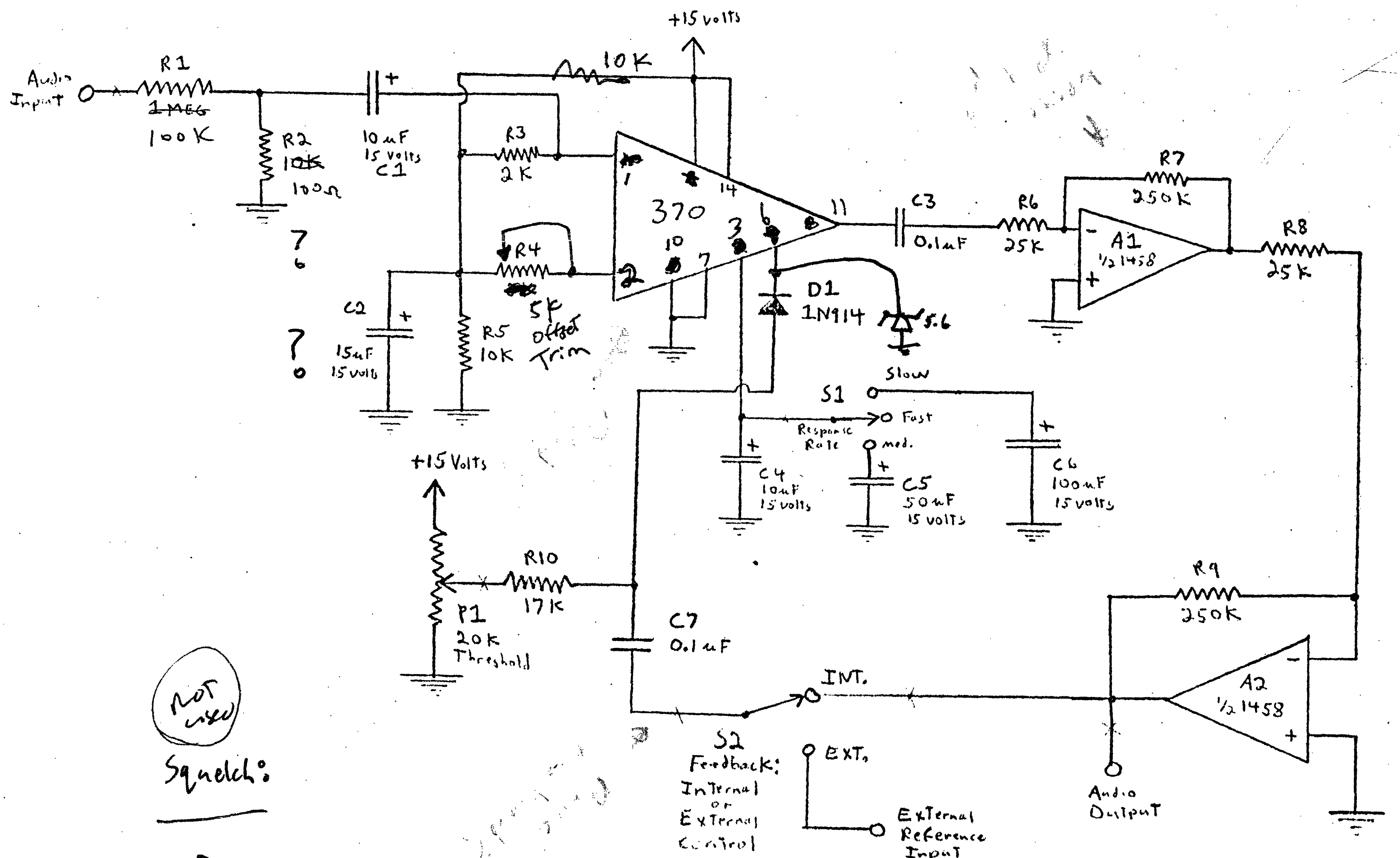
Inputs: Audio input
External control feedback input

Outputs: AGC out

Controls: S1 Control response time (fast/medium/slow)
S2 Control feedback (External/internal)
P1 AGC Threshold

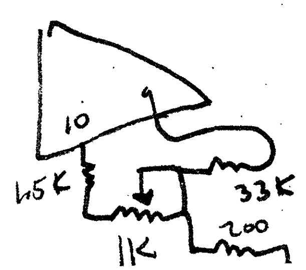
Uses: This module will hold the level of an input constant sith a variable response time. When it is fed back through resonant amplifiers, it produces interesting bird-like chirp sounds. Uses the LM370 chip.

AGC (Automatic Gain Control)



Not used

Squelch:

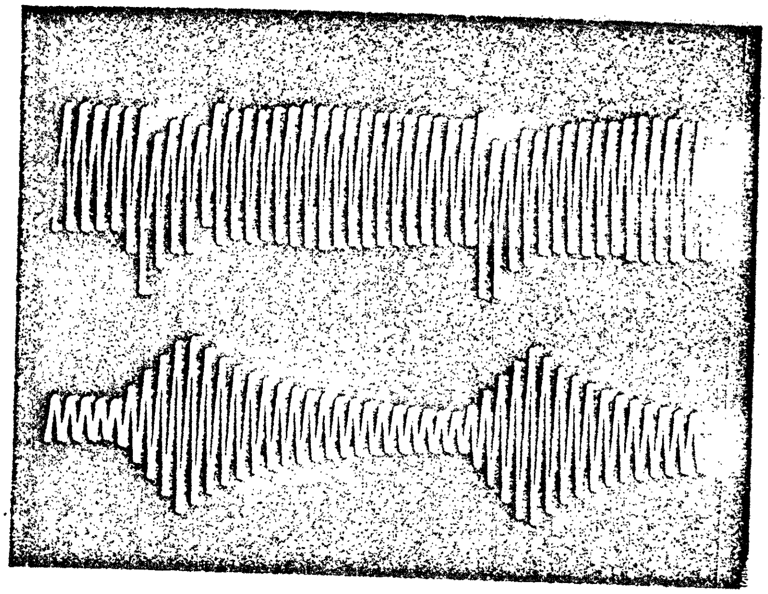


---AGC---

The audio input is attenuated by divider R1/R2 and fed into the input of the LM370 AGC. C1 and C2 isolate and by-pass the input. The squelch threshold is set by P1 and the response rate is selected by S1. The output of the 370 is brought back to its original level via amplifiers A1 and A2. S2 allows us to internally bridge the feedback loop, or close it externally. Because of the large gains involved, this circuit is highly susceptible to noise.

References:

1974 National Semiconductor Linear Applications Handbook



AGC output

Audio wave input to the AGC

Photo#47 - Input of AGC vs. output
As you can see, it does hold the level fairly constant (the control damping is evident).

30) STEREO OUTPUT SECTION

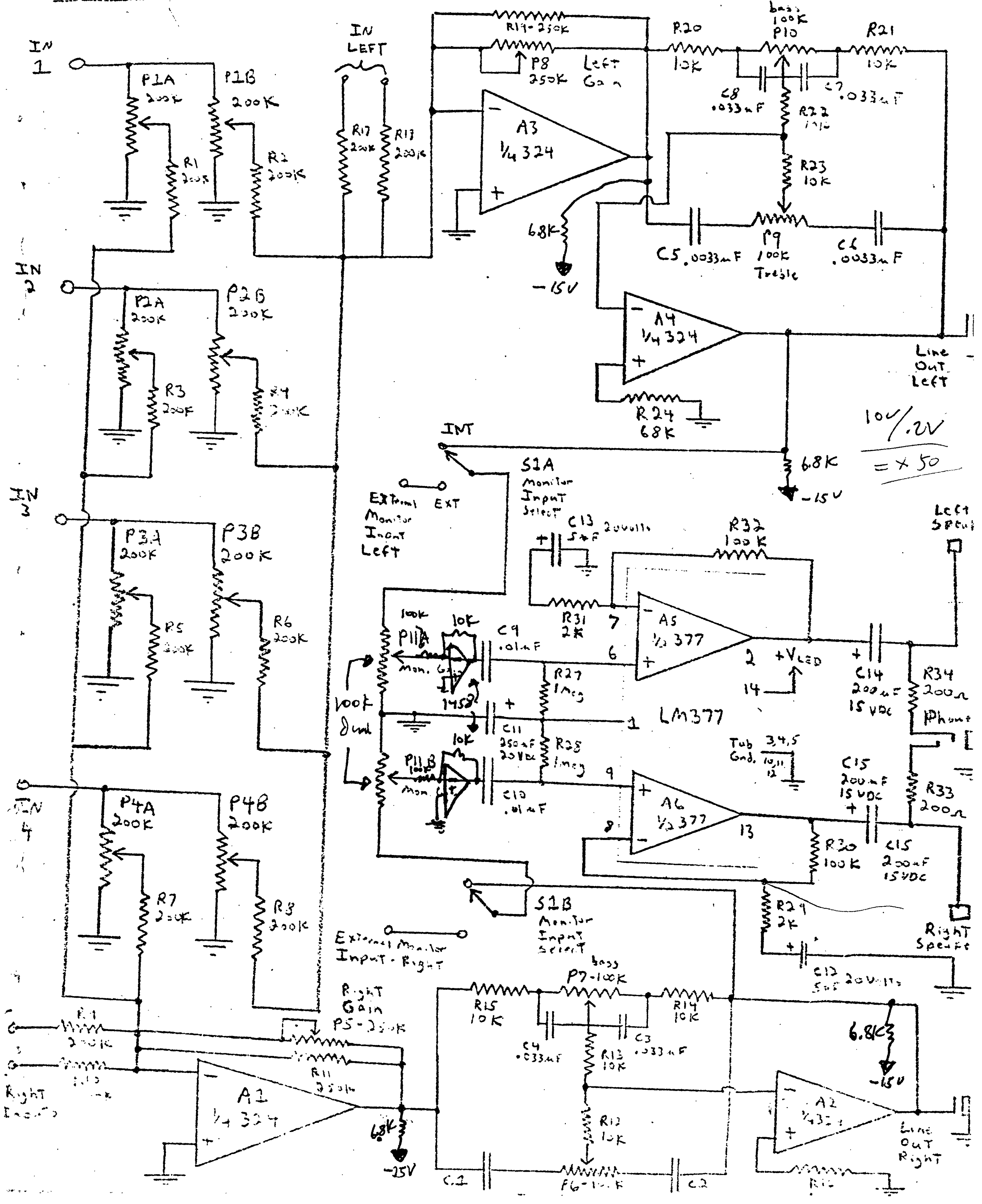
Inputs:
- 4 Left/Right mixable inputs
- 2 Left channel only inputs
- 2 Right channel only inputs
- \- Left monitor external input
- \- Right monitor external input

Outputs:
Low Level (about 1-5 volts p-p) audio outputs, right and left
Monitor output (8 ohm speakers, right and left)
Stereo headphoned (driven by monitor)

Controls:
P1-P4 Left/right mix for the 4 mixable inputs
P6,P7,P9,P10 Seperate Bass/Treble equalization for each channel
P8 Master left output gain
P5 Master right output gain
P11 Monitor output volume
S1 Monitor input source (internal/external)

Uses: This presents a convenient means for stereo mixing, and routing audio signals to a power amplifier, tape recorder, etc, Bass/Treble controls allow one to specify the tone contour for each channel. Built-in monitor amplifier can drive stereo headphones and external 8 ohm monitor speakers. (Uses the LM377 2 watt stereo amplifier.)

STereo OuTput Section



---Stereo Output Section---

Audio inputs 1-4 are scaled by P1-P4, and routed to the left (A3) or right (A4) summer. Auxilary left channel inputs can be mixed in through R17 and R18, while auxilary right channel inputs can be mixed through R9 and R10. The master gains are controlled via P5 (right) and P8 (left). The mix for each channel is fed into filter networks centered around A2 and A4. These allow one to put high/low pass filters into the input or feedback sections of the amplifiers (determined by the potentiometers P6, P7, P9, P10). Thus we have seperate control over the "bass-treble" contour and frequency characteristics of each channel.

The low-level output of these amplifiers may be tapped at the phone jacks for driving external amplifiers, tape recorders, etc. The line outputs are fed via S1 and P11 to the LM377 two watt stereo amplifier. The gain of the 377 is set by the R31/R32 and R29/R30 feedback networks. The output of the 377 is isolated via C14 and C15, and fed to optional 8 ohm speakers. R33 and R34 are protection resistors which allow the 377 to also drive stereo headphones. The 377 is not a very good power amplifier, but it is ideal for an interna monitor and headphone driver.

References: 1974 National Semiconductor Linear Applications handbook