DRAPER LABORATORY

MEMO

To: Distribution
From: J. Paradiso
Date: 23 November 1993
Subject: Design and Test of a Simple Peak-Gated Sampler
Number: ESC-93-310

Copies:

In order to efficiently read out the micromechanical hydrophone array and limit the amount of data that must be transferred, it has been suggested that only the peak signal amplitude and corresponding range (i.e. return time) are retained from each hydrophone between pings. These can then be serially output (as in a video raster), after which the entire chip is reset for the next ping and readout cycle. In order to implement such functions on a hydrophone chip containing hundreds or thousands of elements (or on a stacked wafer set bump-bonded to the hydrophone array), the requisite circuits must be of minimal complexity.

The time-varying gain (TVG) function for the μ-mechanical hydrophone may be generated by varying a bias on the hydrophones themselves[1]. Succeeding analog processing must be realized on silicon, however, to occupy minimal volume. For each hydrophone element, this includes a front-end preamp, a balanced demodulator (or full-wave rectifier) followed by a lowpass filter to recover the envelope, and a circuit that both latches the peak signal amplitude and records the corresponding arrival time over a gated interval. This memo describes a simple circuit developed to realize the latter function set.

Relative arrival time may be recorded in several fashions; i.e. a common free-running clock may be latched at the desired instant (a digital solution used in most of today's Time to Digital converters [TDC's]), or an common analog ramp can be sampled (producing a voltage proportional to the sampling gate delay; an analog solution used in earlier TDC's). The latter technique, which ideally would involve less noise injection and complexity, has been suggested for implementation in the hydrophone array.

An analog circuit to sample one signal at the peak value of another has already been developed and fielded in tests of the Backgammon sonar system[2]; see Fig. 1. This circuit worked quite well up to frequencies approaching 80 Khz, and has been used to quickly calibrate and adjust the Backgammon system. It has been mainly realized from comparitor and operational amplifier circuits, however, and is somewhat complex. As seen in the block diagram of Fig. 2, a comparitor fires whenever the input of the master sample/hold is greater than its output. This is ANDed with a gate derived from the differentiated signal (to insure a rising level), and applied to the sample input of the sample/hold. This gate can be used to drive other sample/hold circuits, allowing multiple signals to be latched at the peak value of the master. The circuit must be re-set at the beginning of each range gate; this is accomplished by briefly pulsing the sample gates at the range gate initiation, as indicated in Fig. 2.

As sketched in Fig. 1, this circuit is far too complicated to realize at each hydrophone element in a μ-mechanical array. Fig. 3, however, depicts a much simpler 2-transistor implementation of the core function. Here, the hydrophone signal is input to the base of transistor Q1, which charges capacitor C1 at its emitter. Looking only at the base-emitter circuit of Q1, this is effectively a conventional peak detector circuit. As C1 charges, however, collector current will flow through Q1, causing Q2 to conduct, and pulling its collector high. Thus a gate is provided at the collector of Q2, which is asserted whenever the capacitor is charging; i.e. whenever the hydrophone signal exceeds its previous level.

Q3 is a switch to reset the peak-hold capacitor C1, and Q4 is a source-follower to buffer the voltage at C1. Q5 and Q6 form a sample-hold circuit to latch the ramp voltage. The circuit diagram of Fig. 3 only suggests the basic concept; an actual design must be adapted to the desired fabrication process and array readout architecture; i.e. a CMOS process such as employed in an analog memory cell [3] may be most appropriate.

Fig. 4 shows a circuit that was actually constructed to demonstrate this design in operation. The additional circuitry of Fig. 4 was inserted for test purposes; i.e. Q3 and Q4 will reset the peak detection capacitor whenever the base of Q4 goes low, the LF351 is a high-impedance buffer amplifier to allow the peak to be recorded without droop, and a conventional sample/hold IC was used to latch an input ramp to determine the relative peak time. The buffer amplifier, sample/hold, and reset switch can be easily realized on a monolithic with JFETs or MOSFETs; the devices shown here were only chosen for convenience (as they were available from previous projects or at the Draper stockroom).

The diode at the emitter of Q1 was inserted to avoid problems with leakage current and base-emitter breakdown, which began to occur in this device for large input swings. This component may be avoided by appropriately fabricating Q1, and tailoring it to the expected signal levels. The two diode junctions in the base circuit of Fig. 4 produce a dead-zone of roughly 1.2 volts above ground before the diodes conduct and the peaks are detected. This can be avoided by resetting the capacitor to a level that is at least 1.2 volts below the minimum input signal. The 1000 pf capacitor used to hold the peak here is very large for a monolithic; a much smaller value should be able to be employed if appropriate modifications are explored.

Again, the component selection was not optimized; the design of Fig. 4 arose from what was on hand, and served only to demonstrate basic function and act as a proof-of-concept. As it stands, this circuit works decently at frequencies above 10 Khz. To make it operate sufficiently in the desired vicinity of 100 Khz, the basic component selection and design must be appropriately reviewed and tweaked. This can be accomplished for a monolithic implementation using VLSI simulation and design tools.

Figs. 5-8 show some test results produced from the circuit of Fig. 4. Fig. 5 shows the ramp and reset input waveforms used in all tests; the reset pulse occurs at the reset of the ramp, and the sensitive duration between resets is 3.8 ms.

The lower portions of the traces in Fig. 6 show the peak detector outputs (i.e. the buffered peak capacitor voltage) for various phases of an input waveform shown on the upper trace. The peak detector voltage is seen to track the positive peaks of the input signal, as expected.

Fig. 7 shows the sample gate signals for an analogous set of input waveforms. These are seen to be synchronous with the changes in peak level. The small changes in peak level occurring near the maximum envelopes are not well detected by this circuit, however; this is because the collector currents of Q1 are not always large enough to turn on Q2 in this vicinity, producing missing or narrow (i.e. top left figure) gate pulses. An optimization of this circuit design (i.e. an increase in the collector resistance, or incorporating Q1,Q2 as a driven cascode) should be able to alleviate the bulk of this problem; the circuit is essentially based on detecting collector current in Q1.

Fig. 8 shows the output of the sample/hold that acquires the ramp (Fig. 5), again for various input waveforms. One can see that this signal increases in amplitude with the relative latency of the input peak, as expected. The effect noted above can be also seen here however; the absolute peak is not latched because of the narrow (i.e. below the minimum aperture time of the sample/hold) or missing sample gate.

Gated Peak Denominator Ratio Generator (October, 1991)

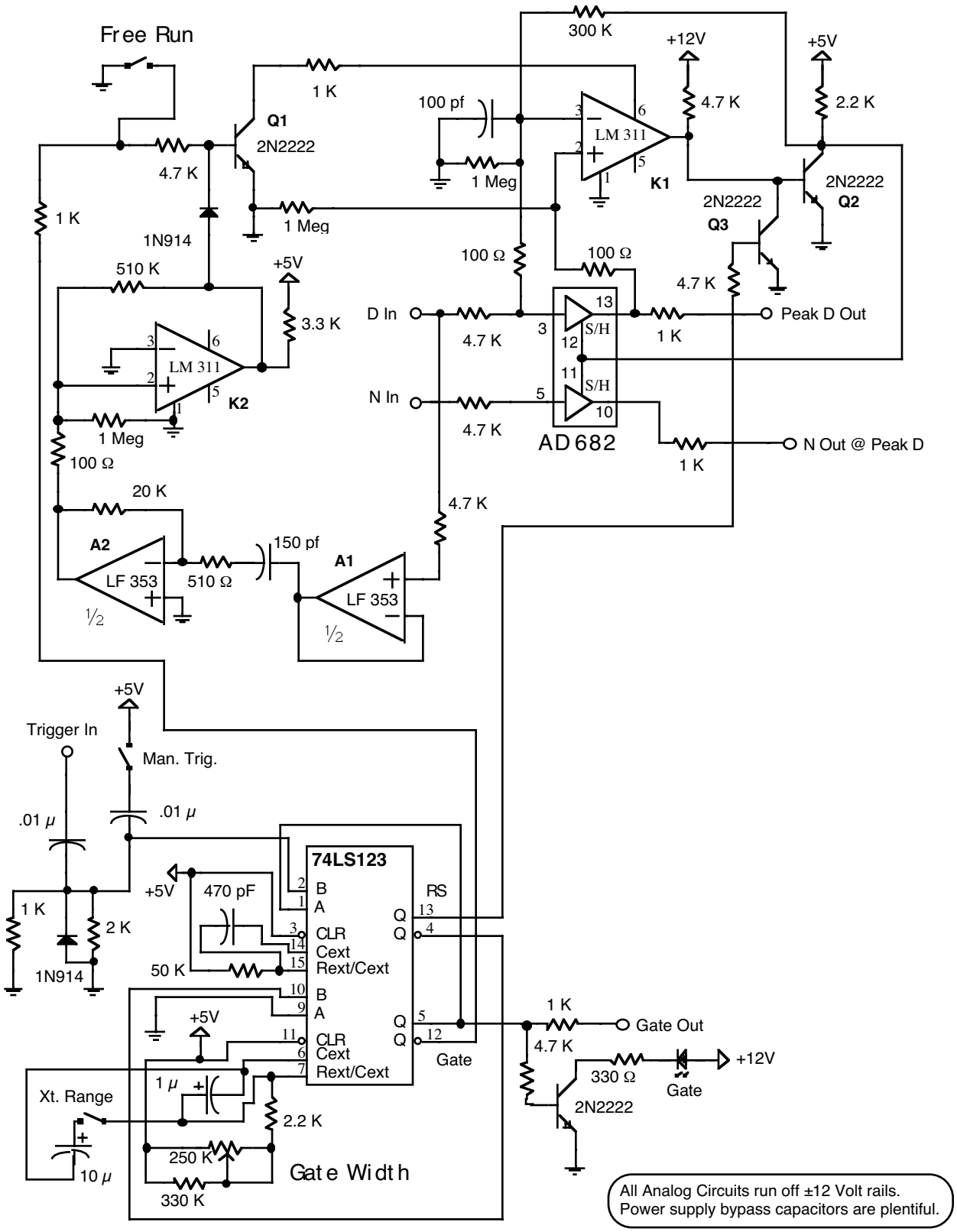

Fig. 1: Peak-Gated Sampler used with the Backgammon Sonar System

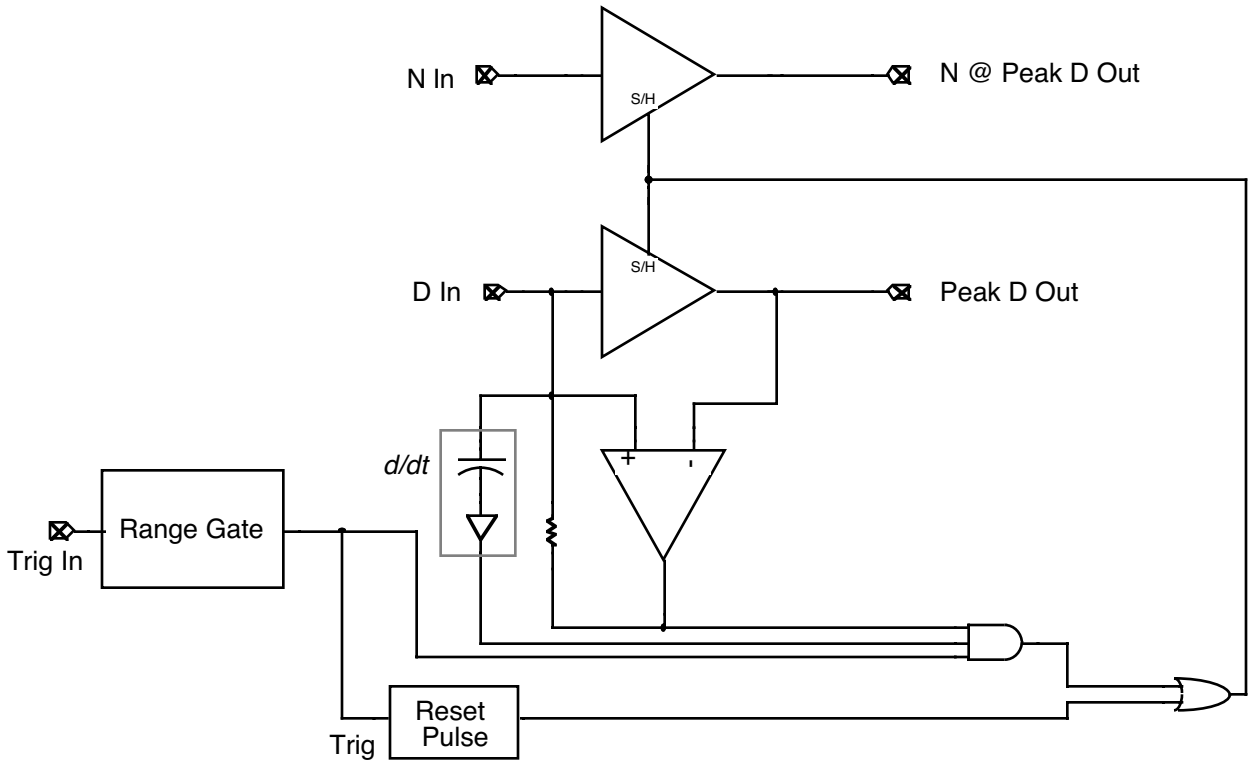

Fig. 2: Block Diagram of the Backgammon Peak Sampler System

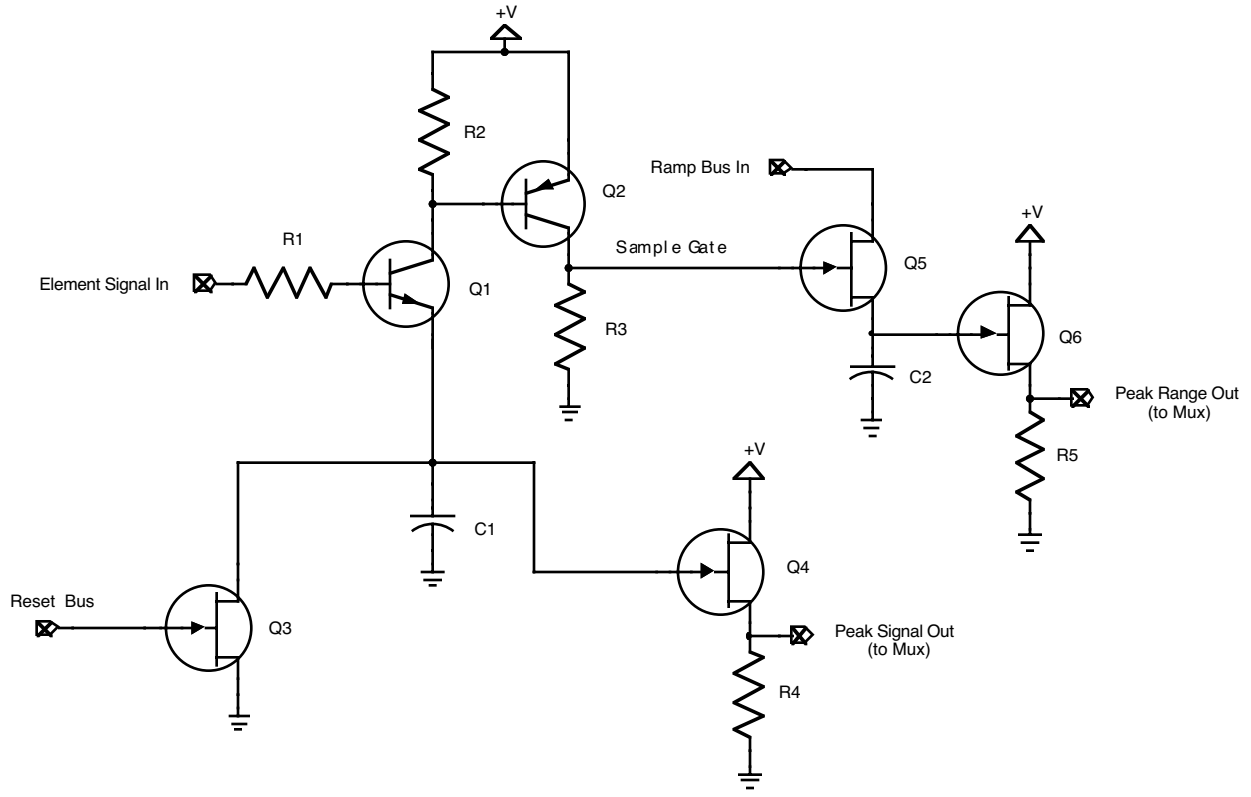

Fig. 3: Design Principle for a Simplified Peak Sampler

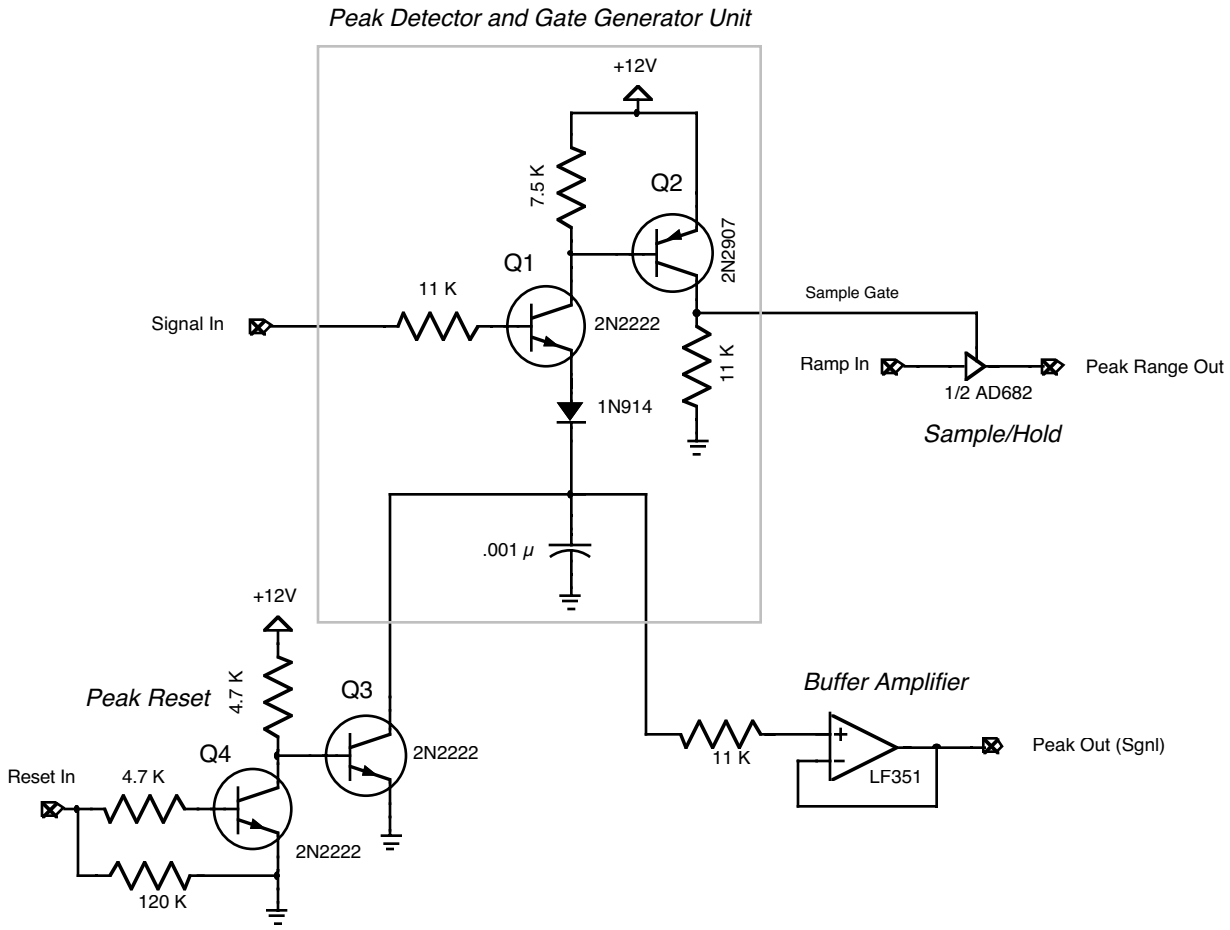

Fig. 4: Peak Sampler Circuit Constructed for Tests

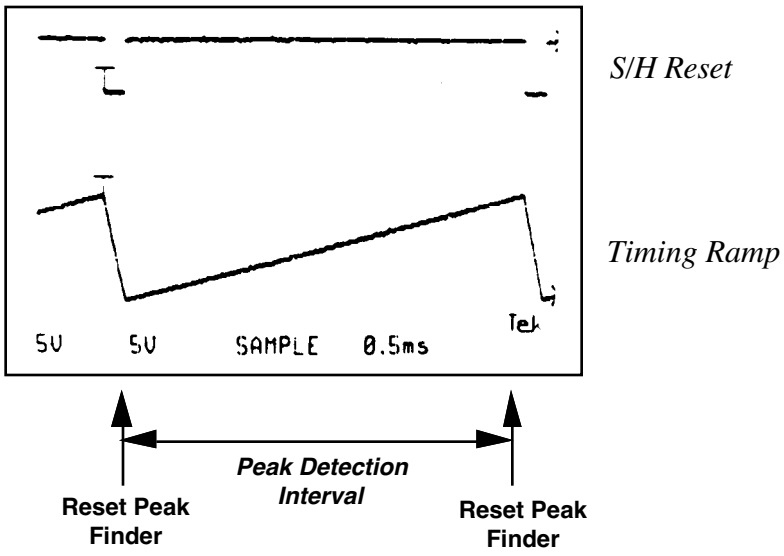

Figure 5: S/H Input Ramp and Reset Signal used in Tests

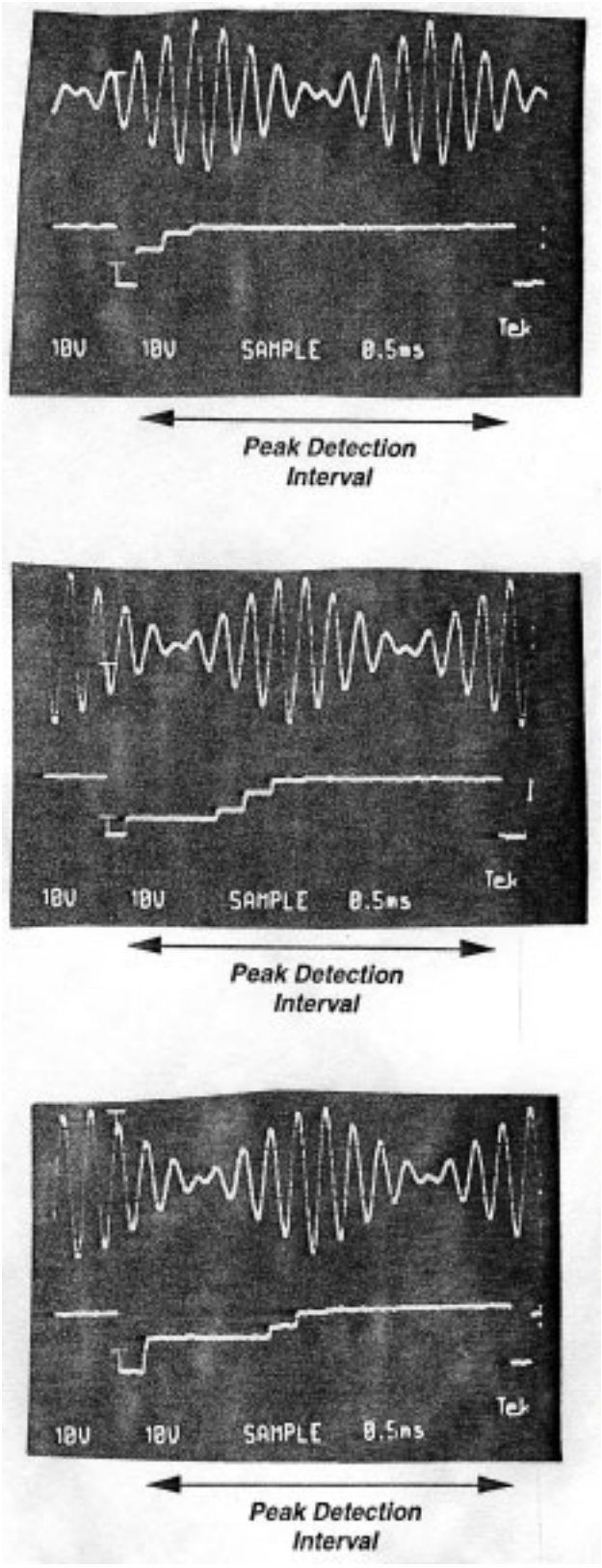

Figure 6: Peak Detector Outputs for Various Input Waveforms

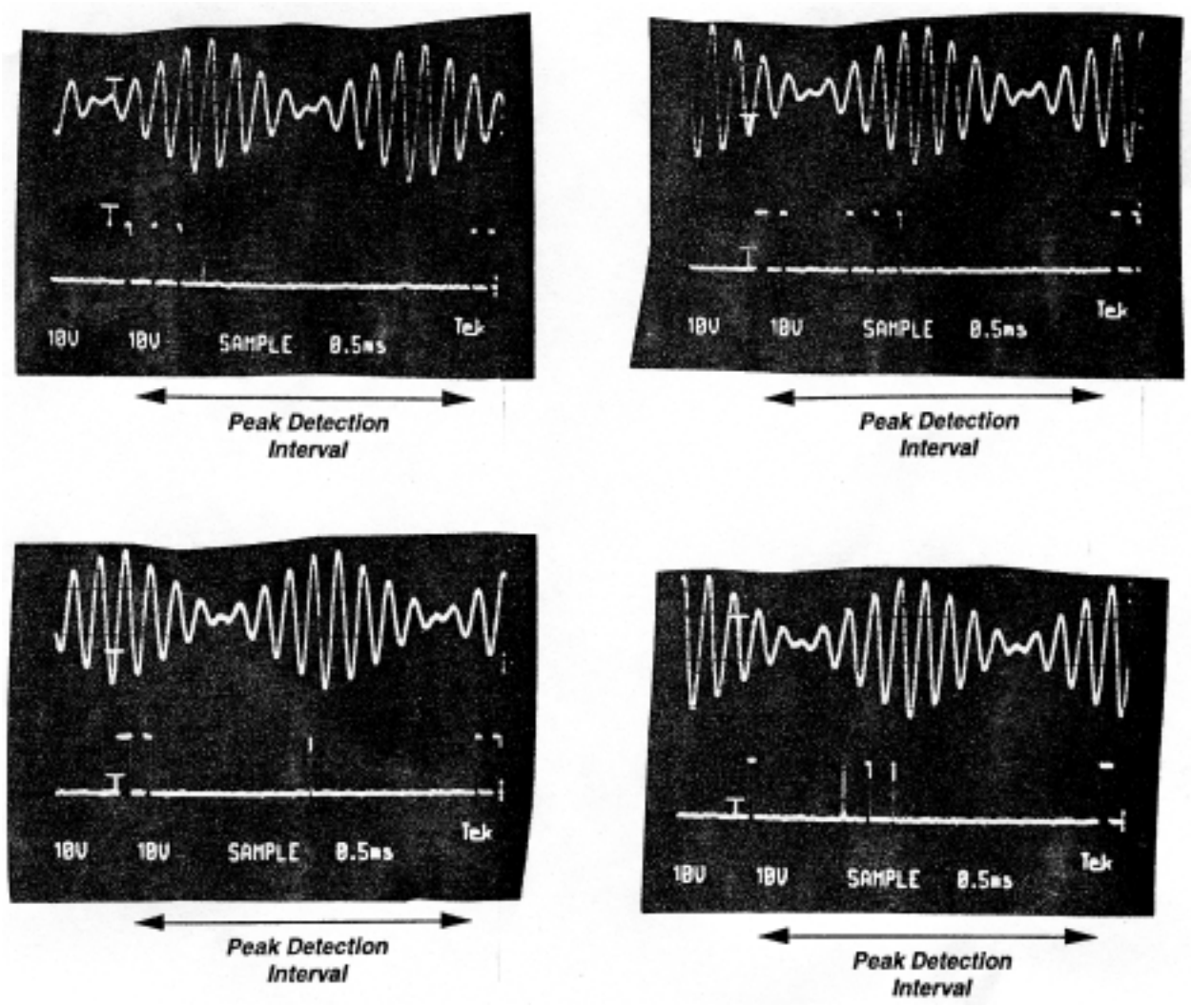

Figure 7: Sample Gate Output for Various Input Waveforms

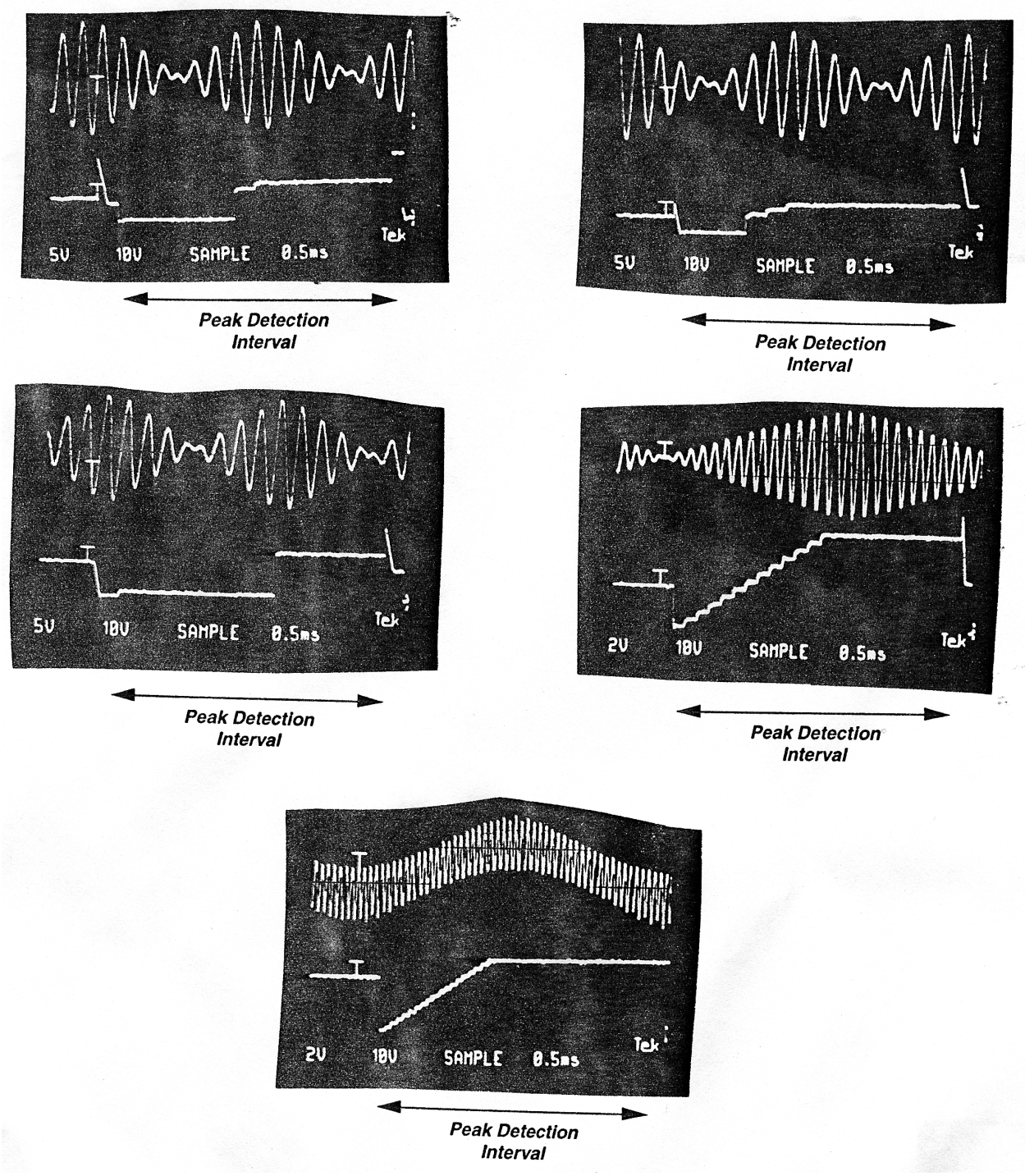

Figure 8: Sampled Ramp (at Peak) for Various Input Waveforms

References

1) Bernstein, J., Rosenstrach, P., "System Study of a Hand-Held High Resolution Acoustic Lens Sonar Using a Micromechanical Hydrophone Retina", EMD-91-267, December 12, 1991.

2) Paradiso, J., "Backgammon Electronics; Past, Present, & Future", EJC-91-1100, October 13, 1991.

3) Jarron, P., "Analog Sampling Techniques in CMOS Technology for Future Front Ends", Proceedings of the First Annual Conference on Electronics for Future Colliders, LeCroy Corporation, Chestnut Ridge, NY, May 22-23, 1991.